RCA

Data Book

Advanced CMOS Logic ICs

GE/RCA/INTERSIL
SEMICONDUCTORS

RCA Advanced CMOS Logic Integrated Circuits

This Data Book contains detailed technical information on the broad line of RCA AC/ACT series of Advanced CMOS Logic integrated circuits. These products match bipolar FAST* in speed, performance, and logic-type output drive, but at CMOS power levels.

The first section, **Product Selectors,** supplies a complete index to devices, selection guide, classification chart, cross-reference guide, packages, and ordering information.

Subsequent sections provide a complete, detailed discussion of Advanced CMOS Logic including **Technical Overview, System Design,** and a description of AC/ACT **Behavioral Models,** called SmartModels**, available to system design engineers for use in board-level simulations. The discussion also covers **Printed-Circuit-Board Design** using AC/ACT devices, AC/ACT **Reliability,** and the availability of **Enhanced Product.**

The **Technical Data** section provides definitive ratings and characteristics data for individual types in the RCA AC/ACT Advanced CMOS Logic product line.

The **Military and Aerospace ICs** section covers the AC/ACT types that are processed and screened in accordance with military and internal high-reliability specifications to meet the demands of modern military, aerospace, and critical industrial and scientific applications.

Next, the new RCA **FCT Bus-Interface Family** of products for use with modern high-speed backplanes are introduced. Features, benefits, ratings and characteristics, output capabilities, and preliminary switching-speed limits are provided.

The Data Book also contains **Dimensional Outlines** and **Application Notes** on the RCA AC/ACT and FCT families of products.

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.
**SmartModel is a Registered Trademark of Logic Automation, Inc.

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GE/RCA/Intersil Semiconductors

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CD74AC646EN/M	CD54AC646H	CD74ACT646EN/M	CD54ACT646H	300	Octal Bus Transceiver/Register, 3-State	24
CD74AC647EN/M	CD54AC647H	CD74ACT647EN/M	CD54ACT647H	307	Octal-Bus Transceiver/Register with Open Drain, Non-Inverting	24
CD74AC648EN/M	CD54AC648H	CD74ACT648EN/M	CD54ACT648H	300	Octal Bus Transceiver/Register, 3-State, Inverting	24
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CD74AC7060E/M	CD54AC7060H	CD74ACT7060E/M	CD54ACT7060H	329	14-Stage Binary Counter with Oscillator	20
CD74AC7061E/M	CD54AC7061H	CD74ACT7061E/M	CD54ACT7061H	329	14-Stage Binary Counter with Oscillator	20
CD74AC7201E/M	CD54AC7201H	CD74ACT7201E/M	CD54ACT7201H	335	512 x 9-Bit Parallel FIFO	28
CD74AC7202E/M	CD54AC7202H	CD74ACT7202E/M	CD54ACT7202H	335	1024 x 9-Bit Parallel FIFO	28
CD74AC7623E/M	CD54AC7623H	CD74ACT7623E/M	CD54ACT7623H	336	Octal-Bus Transceiver, 3-State (B Side), Open-Drain (A Side), Non-Inverting	20
—	—	CD74ACT7651EN/M	CD54ACT7651H	342	Octal-Bus Transceiver/Register, 3-State, Inverting	24

†Package Suffix
- E - Dual-In-Line Plastic
- EN - Dual-In-Line Narrow-Body Plastic
- M - Small-Outline Plastic
- H - Chip

Product Selection Guide

Type	Function/Description	Classification	Page
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	AND/OR/EXCLUSIVE-OR Gates		
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AC/ACT32	Quad 2-Input OR Gate	SSI	105
AC/ACT86	Quad 2-Input EXCLUSIVE-OR Gate	SSI	115
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AC/ACT241	Octal Buffer/Line Driver; 3-State	MSI	200
AC/ACT244	Octal Buffer/Line Driver; 3-State	MSI	200
AC/ACT540	Octal Buffer/Line Driver; 3-State; Inverting	MSI	274
AC/ACT541	Octal Buffer/Line Driver; 3-State	MSI	274
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AC/ACT374	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State	MSI	267
AC/ACT534	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State; Inverting	MSI	267
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AC/ACT323	8-Bit Universal Shift/Storage Register; 3-State; Synchronous Reset	MSI	251
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AC/ACT153	Dual 4-Input Multiplexer	MSI	143
AC/ACT157	Quad 2-Input Multiplexer	MSI	149
AC/ACT158	Quad 2-Input Multiplexer; Inverting	MSI	149
AC/ACT238	3-to-8-Line Decoder/Demultiplexer	MSI	126
AC/ACT251	8-Input Multiplexer; 3-State	MSI	212
AC/ACT253	Dual 4-Input Multiplexer; 3-State	MSI	218
AC/ACT257	Quad 2-Input Multiplexer; 3-State; Non-Inverting Outputs	MSI	224
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Product Classification Chart

GATES

Single-level

NOR/NAND

CD54/74AC/ACT

AC/ACT02
AC/ACT00
AC/ACT10
AC/ACT20

OR/AND/Exclusive-OR

CD54/74AC/ACT

AC/ACT08
AC/ACT32
AC/ACT86

Multi-level

Buffers Line-Drivers

CD54/74AC/ACT

AC/ACT240
AC/ACT241
AC/ACT244
AC/ACT540
AC/ACT541

Bus Drivers

CD54/74AC/ACT

AC/ACT240
AC/ACT241
AC/ACT244
AC/ACT540
AC/ACT541

Inverters

AC/ACT04
AC/ACT05●

Decoders/Encoders

CD54/74AC/ACT

AC/ACT138
AC/ACT139
AC/ACT238

Schmitt Trigger

CD54/74AC/ACT

AC/ACT14

MULTIVIBRATORS

Flip-Flops/Latches

Flip-Flops

CD54/74AC/ACT

AC/ACT74
AC/ACT109
AC/ACT112
AC/ACT174
AC/ACT175
AC/ACT273
AC/ACT374
AC/ACT534
AC/ACT564
AC/ACT574

Latches

CD54/74AC/ACT

AC/ACT373
AC/ACT533
AC/ACT563
AC/ACT573

REGISTERS

Shift

CD54/74AC/ACT

AC/ACT164
AC/ACT299
AC/ACT323

FIFO Buffer

CD54/74AC/ACT

AC/ACT7201
AC/ACT7202

COUNTERS

Synchronous

CD54/74AC/ACT

AC/ACT161
AC/ACT163
AC/ACT191
AC/ACT193
AC/ACT7060
AC/ACT7061

MULTIPLEXERS/DEMULTIPLEXERS

CD54/74AC/ACT

AC/ACT138
AC/ACT139
AC/ACT151
AC/ACT153
AC/ACT157
AC/ACT158
AC/ACT238
AC/ACT251
AC/ACT253
AC/ACT257
AC/ACT258

INTERFACE CIRCUITS

Bus Transceivers

CD54/74AC/ACT

AC/ACT245
AC/ACT623
AC/ACT646
AC/ACT647●
AC/ACT648
AC/ACT649●
AC/ACT651
AC/ACT652
AC/ACT653●
AC/ACT654●
AC/ACT7623●
AC/ACT7651

ARITHMETIC CIRCUITS

Adders/Comparators

CD54/74AC/ACT

AC/ACT283

Parity Generator/Checker

AC/ACT280

PHASE-LOCKED LOOP

CD54/74AC/ACT

AC/ACT297

● Open Drain (one side)

Cross-Reference Guide

Industry Type	RCA Replacement Type	Industry Type	RCA Replacement Type
74AC00P	CD74A0C00E	74AC00S	CD74AC00M
74AC02P	CD74AC02E	74AC02S	CD74AC02M
74AC04P	CD74AC04E	74AC04S	CD74AC04M
74AC05P	CD74AC05E	74AC05S	CD74AC05M
74AC08P	CD74AC08E	74AC08S	CD74AC08M
74AC10P	CD74AC10E	74AC10S	CD74AC10M
74AC14P	CD74AC14E	74AC14S	CD74AC14M
74AC20P	CD74AC20E	74AC20S	CD74AC20M
74AC32P	CD74AC32E	74AC32S	CD74AC32M
74AC74P	CD74AC74E	74AC74S	CD74AC74M
74AC86P	CD74AC86E	74AC86S	CD74AC86M
74AC109P	CD74AC109E	74AC109S	CD74AC109M
74AC112P	CD74AC112E	74AC112S	CD74AC112M
74AC138P	CD74AC138E	74AC138S	CD74AC138M
74AC139P	CD74AC139E	74AC139S	CD74AC139M
74AC151P	CD74AC151E	74AC151S	CD74AC151M
74AC153P	CD74AC153E	74AC153S	CD74AC153M
74AC157P	CD74AC157E	74AC157S	CD74AC157M
74AC158P	CD74AC158E	74AC158S	CD74AC158M
74AC161P	CD74AC161E	74AC161S	CD74AC161M
74AC163P	CD74AC163E	74AC163S	CD74AC163M
74AC164P	CD74AC164E	74AC164S	CD74AC164M
74AC174P	CD74AC174E	74AC174S	CD74AC174M
74AC175P	CD74AC175E	74AC175S	CD74AC175M
74AC191P	CD74AC191E	74AC191S	CD74AC191M
74AC193P	CD74AC193E	74AC193S	CD74AC193M
74AC238P	CD74AC238E	74AC238S	CD74AC238M
74AC240P	CD74AC240E	74AC240S	CD74AC240M
74AC241P	CD74AC241E	74AC241S	CD74AC241M
74AC244P	CD74AC244E	74AC244S	CD74AC244M
74AC245P	CD74AC245E	74AC245S	CD74AC245M
74AC251P	CD74AC251E	74AC251S	CD74AC251M
74AC253P	CD74AC253E	74AC253S	CD74AC253M
74AC257P	CD74AC257E	74AC257S	CD74AC257M
74AC258P	CD74AC258E	74AC258S	CD74AC258M
74AC273P	CD74AC273E	74AC273S	CD74AC273M
74AC280P	CD74AC280E	74AC280S	CD74AC280M
74AC283P	CD74AC283E	74AC283S	CD74AC283M
74AC299P	CD74AC299E	74AC299S	CD74AC299M
74AC323P	CD74AC323E	74AC323S	CD74AC323M
74AC373P	CD74AC373E	74AC373S	CD74AC373M
74AC374P	CD74AC374E	74AC374S	CD74AC374M
74AC533P	CD74AC533E	74AC533S	CD74AC533M
74AC534P	CD74AC534E	74AC534S	CD74AC534M
74AC540P	CD74AC540E	74AC540S	CD74AC540M
74AC541P	CD74AC541E	74AC541S	CD74AC541M
74AC563P	CD74AC563E	74AC563S	CD74AC563M
74AC564P	CD74AC564E	74AC564S	CD74AC564M
74AC573P	CD74AC573E	74AC573S	CD74AC573M
74AC574P	CD74AC574E	74AC574S	CD74AC574M
74AC623P	CD74AC623E	74AC623S	CD74AC623M
74AC646P	CD74AC646EN	74AC646S	CD74AC646M
74AC647P	CD74AC647EN	74AC647S	CD74AC647M
74AC648P	CD74AC648EN	74AC648S	CD74AC648M
74AC649P	CD74AC649EN	74AC649S	CD74AC649M
74AC651P	CD74AC651EN	74AC651S	CD74AC651M
74AC652P	CD74AC652EN	74AC652S	CD74AC652M
74AC653P	CD74AC653EN	74AC653S	CD74AC653M
74AC654P	CD74AC654EN	74AC654S	CD74AC654M
74AC7060P	CD74AC7060EN	74AC7060S	CD74AC7060M
74AC7201P	CD74AC7201E	74AC7201S	CD74AC7201M
74AC7202P	CD74AC7202E	74AC7202S	CD74AC7202M
74AC7623P	CD74AC7623E	74AC7623S	CD74AC7623M

Cross-Reference Guide

Industry Type	RCA Replacement Type	Industry Type	RCA Replacement Type
74ACT00P	CD74ACT00E	74ACT00S	CD74ACT00M
74ACT02P	CD74ACT02E	74ACT02S	CD74ACT02M
74ACT04P	CD74ACT04E	74ACT04S	CD74ACT04M
74ACT05P	CD74ACT05E	74ACT05S	CD74ACT05M
74ACT08P	CD74ACT08E	74ACT08S	CD74ACT08M
74ACT10P	CD74ACT10E	74ACT10S	CD74ACT10M
74ACT14P	CD74ACT14E	74ACT14S	CD74ACT14M
74ACT20P	CD74ACT20E	74ACT20S	CD74ACT20M
74ACT32P	CD74ACT32E	74ACT32S	CD74ACT32M
74ACT74P	CD74ACT74E	74ACT74S	CD74ACT74M
74ACT86P	CD74ACT86E	74ACT86S	CD74ACT86M
74ACT109P	CD74ACT109E	74ACT109S	CD74ACT109M
74ACT112P	CD74ACT112E	74ACT112S	CD74ACT112M
74ACT138P	CD74ACT138E	74ACT138S	CD74ACT138M
74ACT139P	CD74ACT139E	74ACT139S	CD74ACT139M
74ACT151P	CD74ACT151E	74ACT151S	CD74ACT151M
74ACT153P	CD74ACT153E	74ACT153S	CD74ACT153M
74ACT157P	CD74ACT157E	74ACT157S	CD74ACT157M
74ACT158P	CD74ACT158E	74ACT158S	CD74ACT158M
74ACT161P	CD74ACT161E	74ACT161S	CD74ACT161M
74ACT163P	CD74ACT163E	74ACT163S	CD74ACT163M
74ACT164P	CD74ACT164E	74ACT164S	CD74ACT164M
74ACT174P	CD74ACT174E	74ACT174S	CD74ACT174M
74ACT175P	CD74ACT175E	74ACT175S	CD74ACT175M
74ACT191P	CD74ACT191E	74ACT191S	CD74ACT191M
74ACT193P	CD74ACT193E	74ACT193S	CD74ACT193M
74ACT238P	CD74ACT238E	74ACT238S	CD74ACT238M
74ACT240P	CD74ACT240E	74ACT240S	CD74ACT240M
74ACT241P	CD74ACT241E	74ACT241S	CD74ACT241M
74ACT244P	CD74ACT244E	74ACT244S	CD74ACT244M
74ACT245P	CD74ACT245E	74ACT245S	CD74ACT245M
74ACT251P	CD74ACT251E	74ACT251S	CD74ACT251M
74ACT253P	CD74ACT253E	74ACT253S	CD74ACT253M
74ACT257P	CD74ACT257E	74ACT257S	CD74ACT257M
74ACT258P	CD74ACT258E	74ACT258S	CD74ACT258M
74ACT273P	CD74ACT273E	74ACT273S	CD74ACT273M
74ACT280P	CD74ACT280E	74ACT280S	CD74ACT280M
74ACT283P	CD74ACT283E	74ACT283S	CD74ACT283M
74ACT299P	CD74ACT299E	74ACT299S	CD74ACT299M
74ACT323P	CD74ACT323E	74ACT323S	CD74ACT323M
74ACT373P	CD74ACT373E	74ACT373S	CD74ACT373M
74ACT374P	CD74ACT374E	74ACT374S	CD74ACT374M
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74ACT534P	CD74ACT534E	74ACT534S	CD74ACT534M
74ACT540P	CD74ACT540E	74ACT540S	CD74ACT540M
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74ACT623P	CD74ACT623E	74ACT623S	CD74ACT623M
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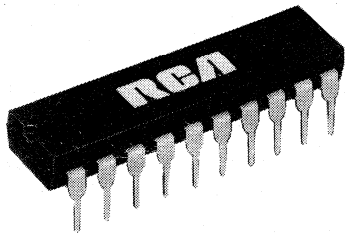
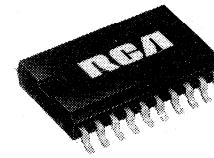
74ACT653P	CD74ACT653EN	74ACT653S	CD74ACT653M
74ACT654P	CD74ACT654EN	74ACT654S	CD74ACT654M
74ACT7060P	CD74ACT7060E	74ACT7060S	CD74ACT7060M
74ACT7201P	CD74ACT7201E	74ACT7201S	CD74ACT7201M
74ACT7202P	CD74ACT7202E	74ACT7202S	CD74ACT7202M
74ACT7623P	CD74ACT7623E	74ACT7623S	CD74ACT7623M

Packages

Typical Dual-In-Line Plastic Package



Typical SO (Small Outline) Plastic Package



Ordering Information

CD **74AC** **245** **E** **X**

RCA Advanced CMOS Digital Logic

Temperature Range Family
- 74AC = Commercial Advanced CMOS
- 54AC = Military Advanced CMOS
- 74ACT = Commercial TTL-Compatible Advanced CMOS
- 54ACT = Military TTL-Compatible Advanced CMOS

Device Type

Package Code
- E = Plastic DIP
- EN = Narrow-Body 24-Lead Plastic DIP
- H = Chip
- M = Small Outline

Special Variation
- X = Burn-in

Temperature Range
All packages when properly derated can be operated from -55 to +125°C.
At low temperature, limit for E and M packages is -55°C.

Package Outlines
The package outlines indicated above are shown in the dimensional outlines section.

2

Technical Overview

FEATURES

The RCA AC/ACT series of Advanced High-Speed CMOS Integrated Circuits is comprised of a broad range of logic types equivalent in performance and speed to FAST, AS (Advanced Schottky), and S (Schottky) bipolar types, but superior in that they require substantially less power in logic operations. Each CMOS circuit function is offered in two basic logic series, as follows:

1. **CD54/74ACTXXX-series types.** These types feature TTL input-voltage-level compatibility and, using the same standardized pin-outs, provide reduced power-consumption alternatives to the very high power consumption of the FAST, AS, and S bipolar logic series types.
2. **CD54/74ACXXX-series types.** These types feature CMOS input-voltage-level compatibility and, using the same standardized pin-outs, provide enhanced system performance (better system noise margin) at speeds similar to those of FAST, AS, and S logic series types.

The AC/ACT family consists of a comprehensive set of octal buffers, octal latches, octal flip-flops, octal transceivers in both the classic 200-series pin-out and the newer 500-series flow-through pin-out. In addition, selected SSI inverters, gates, flip-flops, Schmitt triggers, plus selected MSI counters, registers, multiplexers, decoders, arithmetic functions, and FIFOs are included for well over 100 circuits, in both the ACT and AC series; more types are planned.

AC/ACT Family Features

Following is a listing of the features of the AC/ACT family of logic devices.

- Functionally and pin-compatible with industry 54 and 74 bipolar types in the FAST, AS, and S series
- CMOS rail-to-rail output swing for maximum noise margins
- Fanout (over temperature):
  2400 AC/ACT Loads
  15 FAST Loads
  48 AS Loads
- Wide operating-temperature ranges:
  Plastic (DIP) and Small-Outline 74 series: -55 to +125°C
  chip-form 54 series: -55 to +125°C
  NOTE: FAST, AS and S 74 series types are rated for only 0 to +70°C
- Balanced propagation and output transition times
- Significant power reduction compared to FAST, AS, and S TTL logic, resulting in improved equipment reliability
- Outputs reliably drive 50-ohm lines (at 85°C) and 75-ohms lines (at 125°C) without need for terminations
- Meets JEDEC Standard No. 20; presently, in draft (non-issued) form
- Octal types have typically a 1-volt peak (DIP package) simultaneous switching-voltage transient, similar to FAST series. Peak is typically 0.8 volt in the small-outline package.
- CMOS input compatible

Table I. Performance Comparison of AC/ACT and FAST Logic Functions.

Characteristic	74 Series AC/ACT			74 Series FAST		
1. Power Consumption (mW):	**Frequency (MHz)**			**Frequency (MHz)**		
	0	**1**	**10**	**0**	**1**	**10**
Four-stage counter (191)	0.44	5.5	55	204	224	306
Octal transceiver (245)	0.44	39	390	468	514	702
2. Operating Voltage (volts):	AC: 1.5 to 5.5 ACT: 4.5 to 5.5			4.75 to 5.25		
3. Operating Temperature Range (°C):	-55 to +125			0 to +70		
4. Noise Margin (volts):						
(V_{CC}=4.5 V, rated load)						
FAST to FAST	—			0.4/0.3		
AC to AC (High/Low)	1.25/1.25			—		
ACT to ACT	1.8/0.36			—		
5. Input Switching Voltage Variation over the Operating Temperature Range (mV):	$V_S \pm 50$			$V_S \pm 200$		
6. Output Drive Current (mA):						
(V_{CC}=4.5 V)				(I_{OL}/I_{OH})		
SSI/MSI Logic	±24			+20/-1		
3-State Buffers	±24			+24/-3		
Bus Drivers	±24			+64/-15		
7. Propagation Delay (ns):						
(t_{PHL}/t_{PLH})						
Octal Buffer (240)	7.8/7.8			6/9		
Flip-Flop (74)	9.4/9.4			10.5/8.5		
8. Input Current (μA):						
I_{IL}	+1			+1600		
I_{IH}	-1			-20		
9. Three-State Output Current (μA):	±5			±50		

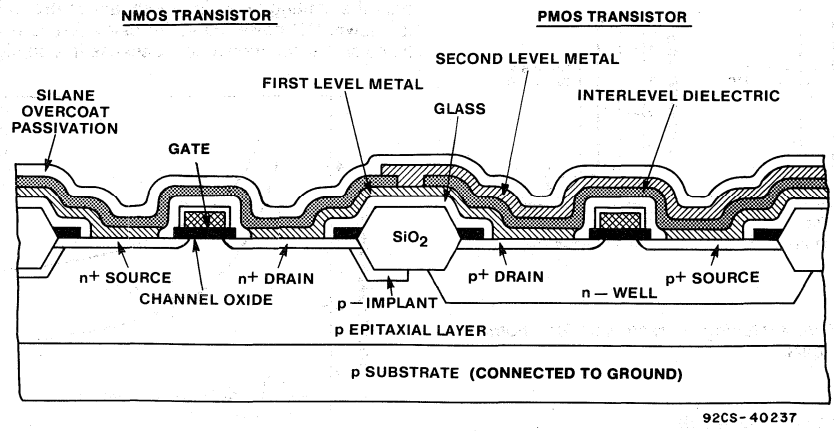


Fig. 1 - Cross section of AC/ACT two-level-metal CMOS process.

Series Features

Following are the special features of the **AC series** of Advanced CMOS High-Speed ICs.

- 1.5- to 5.5-volt operation
- High noise immunity:
  $N_{IL} = N_{IH} = 30\%$ for $V_{CC} = 3$ to 5 volts
  $N_{IL} = N_{IH} = 20\%$ for $V_{CC} = 1.5$ to 3 volts

Following are the special features of the **ACT Series** of Advanced CMOS High-Speed ICs.

- 4.5- to 5.5-volt operation
- Direct TTL input logic compatible:
  $V_{IL} = 0.8$ volt (max); $V_{IH} = 2$ volts (min)
- Similar to FAST specifications except for the 64-milliampere I_{OL} of FAST drivers. (See FCT Series of logic types for higher-current drivers.)

Comparison of AC/ACT Logic Types with FAST/AS Types

RCA AC and ACT types have many outstanding advantages when compared with the conventional high-current bipolar FAST and AS logic types. The Advanced CMOS Logic AC and ACT types can replace the bipolar types in existing equipment and in new equipment designs requiring devices that operate at frequencies up to 100 MHz. Table I compares the significant operating characteristics of the AC and ACT CMOS types with those of the bipolar FAST logic family.

AC/ACT IC Process and Structure

Advanced CMOS high-speed products are fabricated with an advanced small-geometry CMOS process and design rules that are tailored to meet the specified high speed and high output-drive current, and to tame the high switching-current transients associated with high-speed designs. Fig. 1 shows the cross section of an AC/ACT chip. The starting material is a p-substrate topped with a thin p-epitaxial surface layer; hence, this process is an n-well type. The epitaxial surface serves essentially to eliminate SCR latch-up and provides for a low-impedance surface-conduction path that enhances electrostatic discharge capability. The n and p diffusions are ion-implanted. Polysilicon gates having an effective length of 1.5 microns are deposited over a thin 300-angstrom gate oxide. Active source and drain areas are automatically aligned to the separate gates with the polysilicon gates acting as a mask. This structure drastically reduces the parasitic capacitances between the gate and the n and p areas (see Fig. 2) and, as a result, enhances switching speed. The n and p transistors are isolated by the areas of silicon dioxide, as shown in Fig. 1.

A major structural feature of AC/ACT devices is the use of two metallization levels. Logic interconnections are shorter because of the dual interconnect layers, and V_{CC} and ground distribution busing is greatly enhanced to handle the switching transient current, which can exceed one ampere for AC/ACT octal buffer types. When used in chip form, the AC/ACT substrate should not be connected to any potential above ground.

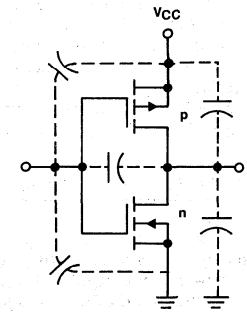


Fig. 2 - Parasitic capacitances in a CMOS inverter.

INPUT CHARACTERISTICS

The inputs of the AC/ACT devices are sensitive to voltage levels. The only input current is the reverse diode leakage (a few picoamperes) of the protection network for electrostatic discharge. The definitive I/O switching characteristics of an input stage is shown in Fig. 3 for AC and ACT types. The specified MIN/MAX input switching voltages are guaranteed over the operating temperature range. Actual shift of the input voltage over the temperature range -55 to +125°C is 100 millivolts.

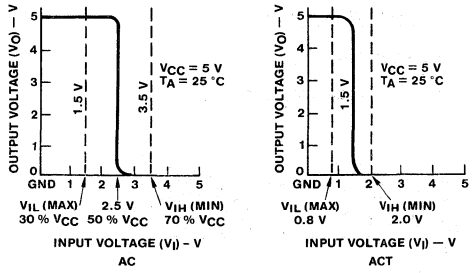


Fig. 3 - AC/ACT I/O switching characteristic for a nominal V_{CC} of 5 volts.

Noise Immunity and Noise Margin

Table II shows the input noise immunity values (V_{IL} max and V_{IH}min) for AC and ACT devices, the output voltage specifications, and the calculated noise margins under two conditions: (1) interfacing with like members of the same family, and (2) interfacing with bipolar FAST types. The noise margins shown in Table II (a), for AC and ACT types only, apply for the temperature range of -55 to +125°C. In Table II (b), the interface noise margins are limited to 0 to +70°C, the commercial temperature range of FAST types. These tables illustrate one of the most important attributes of the CMOS AC/ACT family when compared to the FAST family; namely, designs that use the AC-Series CMOS types have over three times the noise margin of the FAST family in the same design. Hence, new designs taking advantage of the higher speeds of these types should use the 1.4-volt noise margin of the AC family to gain the extra system noise margin of one volt.

Pulsed-input noise immunity is illustrated in Fig. 4. This figure shows the typical family dc noise immunity for input pulses having widths of 10 or more nanoseconds. Below 10 nanoseconds, the pulse amplitude (V_P) reaches higher values before an input is sufficiently disturbed to cause an output change. Note that for AC types, the values are for V_P amplitudes above ground or below V_{CC} (5 volts). For ACT types, only the limiting noise immunity above ground (0.8 volt dc) is shown. DC noise immunity below V_{CC} is 3 volts for ACT types and is not shown here because it is so high.

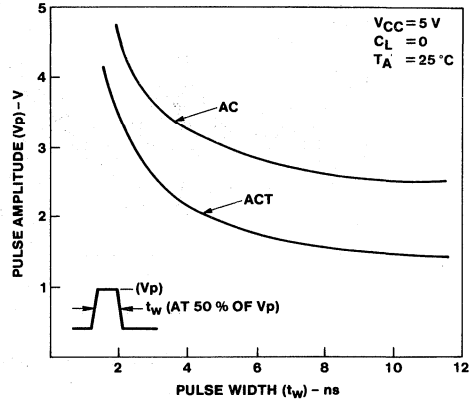


Fig. 4 - Typical dynamic noise immunity.

Input Current/Voltage Characteristic

The inputs of the AC/ACT devices have the dual-diode clamping circuit shown in Fig. 5. This circuit serves two important needs: (1) Ringing voltages above V_{CC} and below ground caused by the RLC interface equivalent circuit are clamped to within one diode drop of V_{CC} and ground, thereby reducing EMI. (2) Electrostatic discharge (ESD) is shunted away from the gate oxide of input transistors. Between -0.5 volt and V_{CC} plus 0.5 volt (see Fig. 6), the input current is typically under the ±1 nanoampere typical leakage of the biased input diodes. Beyond -0.5 volt and V_{CC} plus 0.5 volt, the diodes are forward biased and clamping action begins. The diodes can handle large junction currents (±400 milliamperes for under one second). For continuous clamping action over the operating temperature range, the aluminum input metallization traces are reliably sized for ±20 milliamperes, as shown in Fig. 6. Note that it is the aluminum traces and not the diode junctions that are the limiting circuit elements.

Table II (a). Noise Immunity Values and Noise Margin for AC/ACT Types (V_{CC} = 5 volts).

	AC Types	ACT Types	
Maximum Low-Level Input Voltage (V_{IL} max)	1.5	0.8	volts
Minimum High-Level Input Voltage (V_{IH} min)	3.5	2	volts
Maximum Low-Level Output Voltage (V_{OL} max)	0.1	0.1	volts
Minimum High-Level Output Voltage (V_{OH} min)	4.9	4.9	volts
Noise Margin Low Level (V_{NML})	1.4	0.7	volts
Noise Margin High Level (V_{NMH})	1.4	2.9	volts
NOTE: $V_{NML} = V_{IL}$ max – V_{OL} max $V_{NMH} = V_{OH}$ min – V_{IH} min			

Table II (b). Noise Immunity Values and Noise Margin of AC/ACT Types Driving FAST Types and of FAST Types Driving AC/ACT Types (V_{CC} = 4.5 volts).

	AC/ACT———>FAST		FAST———>AC/ACT		
Maximum Low-Level Input Voltage (V_{IL} max)	—	0.8	—	0.8	volts
Minimum High-Level Input Voltage (V_{IH} min)	—	2	—	2	volts
Maximum Low-Level Output Voltage (V_{OL} max)	0.44	—	0.5	—	volts
Minimum High-Level Output Voltage (V_{OH} min)	3.8	—	2.4	—	volts
Noise Margin Low Level (V_{NML})	0.36		0.3		volts
Noise Margin High Level (V_{NMH})	1.8		0.4		volts

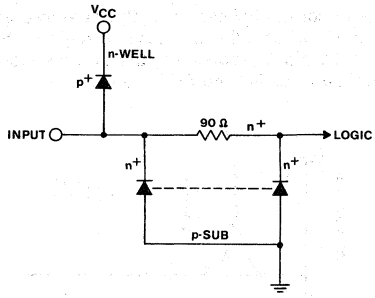


Fig. 5 - AC/ACT dual-diode input protection network.

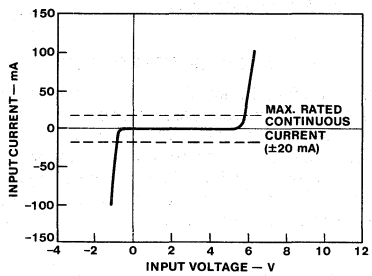


Fig. 6 - AC/ACT input characteristic.

Input Termination

The inputs of all AC/ACT types require termination. The input resistance of these types is very high, typically 10^9 ohms, and the input capacitance is a few picofarads. When unterminated inputs are left floating, they can easily pick up stray charge and move the transistor into the linear operating voltage range between V_{IL} and V_{IH}. When this transfer takes place, logic malfunction could occur, oscillation may occur, and operating current goes up. Consequently, all unused CMOS inputs must be terminated. Terminations may be directly to V_{CC} or to ground or made by means of a shunt resistor. Specification information on input termination design rules is given in the **System Design** section later in this Manual.

Input ESD Protection

As mentioned, AC/ACT device inputs have a resistor-diode protection network, shown in Fig. 5, that protects the gate oxide from electrostatic discharge (ESD) damage. The network provides protection to levels greater than two kilovolts in all modes pertaining to the input, as shown in Fig. 7. This two-kilovolt figure was arrived at by the testing of devices in the ESD test circuit shown in Fig. 8 while conforming to the MIL-STD test requirements. Despite the excellent built-in ESD protection, these device could be exposed to up to 15 kilovolts if good handling practice for semiconductor ICs is not followed. Please refer to RCA ICAN 6525 and ICE 402 for more detailed guidance. One special difference between the RCA AC/ACT logic family and RCA's other CMOS families is the use of P subtrates that are at ground potential (see Fig. 1). The RCA CD4000B and HC/HCT families of logic device use N-substrate material, which is at V_{CC} potential. Because of this difference, the bonding sequence for AC/ACT types is changed so that the ground pin is bonded first. The rule for N-substrate logic is to bond the V_{CC} or V_{DD} pad first.

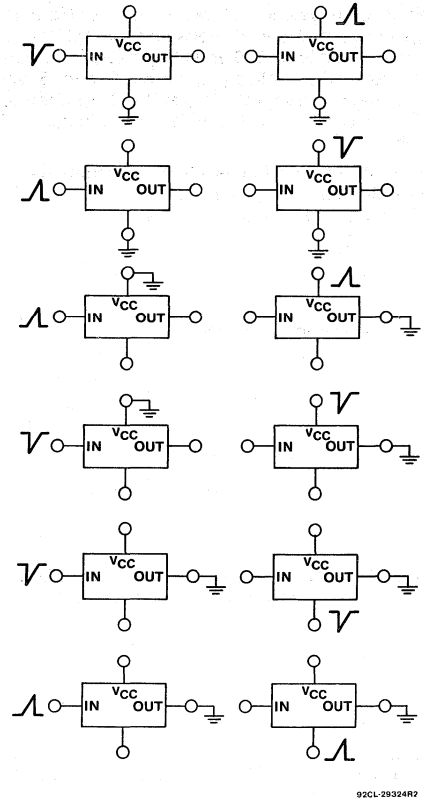


Fig. 7 - Electrostatic discharge (ESD) test modes.

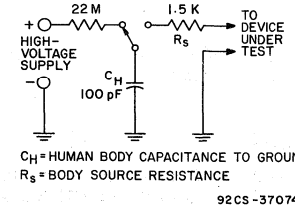


Fig. 8 - Test circuit for measuring electrostatic discharge (ESD) in AC/ACT circuits. The rise time at the output terminal should be 13 ± 2 ns.

Input Interaction

Another effect of the input-protection network is the imposition of a parasitic transistor between adjacent input pins. Fig. 9 shows this transistor. This parasitic transistor action may cause undesirable interaction between adjacent inputs if the input level is less than ground. In AC/ACT devices, gain of the transistor (alpha = I_C/I_E) is minimized to less than 0.001, thereby permitting proper logic operation in the presence of large below-ground transient voltages.

An application example in which the knowledge that alpha equals 0.001 is useful is shown in Fig. 10. Here, if input A swings between -5 and +5 volts and the AC/ACT device is operated normally from 5 volts to ground, it is wanted that the output switch reliably between 0 and 5 volts. The designer must consider the V_{ILB} at the B input terminal. Calculations show that this is a safe design, because V_{ILB} = 4.3 millivolts.

I_E = 4.3 volts/20 kilohms = 0.215 milliamperes
$I_C = \alpha I_E$ = 0.215 microamperes
$V_{ILB} = I_C$ x 20 kilohms = 4.3 millivolts

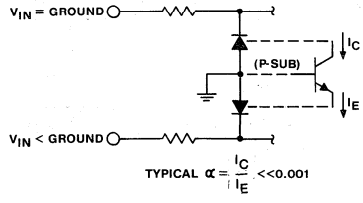


Fig. 9 - Parasitic n-p-n transistor between adjacent pins imposed by input protection network.

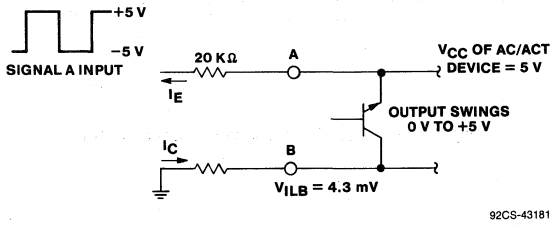


Fig. 10 - Example of use of input interaction (a) in a level conversion.

Input Capacitance

The input capacitance C_I as a function of input voltage is shown in Fig. 11 for typical AC and ACT types. Note that C_I has peak values at the respective input-voltage switch point of 1.5 volts for ACT and 2.5 volts for AC types. Capacitance on either side of the peak is a summation of package, leadframe, reverse-biased input diode, and CMOS gate-to-source/drain capacitance. The peak capacitance results from the Miller-effect multiplication of the gate-to-drain capacitance in the high-gain linear-transition region. The value of C_I that most typically represents the average loading effect is 5.0 picofarads for AC and ACT inputs.

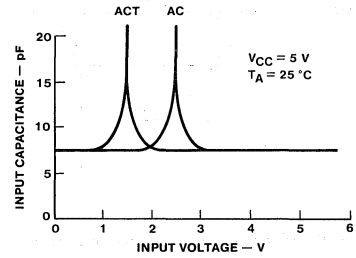


Fig. 11 - Variation of input capacitance with voltages for typical AC/ACT types.

LATCH-UP SENSITIVITY

Latch-up is a state in which an unwanted low-impedance path develops in a parasitic four-stage bipolar structure in a CMOS IC. Latch-up may be initiated or triggered by voltage overshoot or undershoot at inputs, outputs, or supply terminals. A high transient voltage or current at any one terminal or at any combination of these terminals may initiate turn-on of the parasitic SCR-type four-layer diode bipolar device. See Fig. 12 (a).

A simplified diagram of this parasitic structure is shown in Fig. 12 (b). This structure, when triggered on, keeps the supply voltage below the V_{CC} voltage value and thus permits a high supply current of several hundred milliamperes to flow [see I_C in Fig. 12 (b)]. The values of resistors R_p and R_n depend on the circuit layout geometry and on p+ and n+ doping levels. The lower the value of these resistors, the less the voltage drop that will occur and the higher the trigger current needed to induce turn-on of the SCR structure.

Also important for minimizing latch-up problems are the established layout rules and process parameters that minimize the current gain (beta) of the parasitic n-p-n and p-n-p transistors shown in Fig. 12.

The RCA AC/ACT n-well process uses a thin p-epitaxial layer on the p+ substrate. This layer provides a shunt of very low resistance around R_p. The effective R_p is extremely low, and as a result, very high negative voltage or current transients at the n+ source (V_{SS} point in Fig. 12) are required to forward bias the parasitic n-p-n base-emitter junction. Additionally, there are several design rules that also significantly decrease latch-up probability. These rules relate to:

1. Layout spacings to reduce the parasitic n-p-n and p-n-p transistor current gain
2. n+/n-well doping
3. Closed structure outputs
4. Latch plugs liberally used

The current transient at any input or output terminal that could potentially trigger latch-up of AC/ACT ICs is typically more than ±400 milliamperes at 25°C. Measurements are made at all terminals to assure that they have a latch current of over ±100 milliamperes at 125°C. The absolute maximum dc rating in AC/ACT data sheets and in the proposed industry JEDEC Standard No. 20 is ±20 milliamperes at inputs and ±50 milliamperes at outputs.

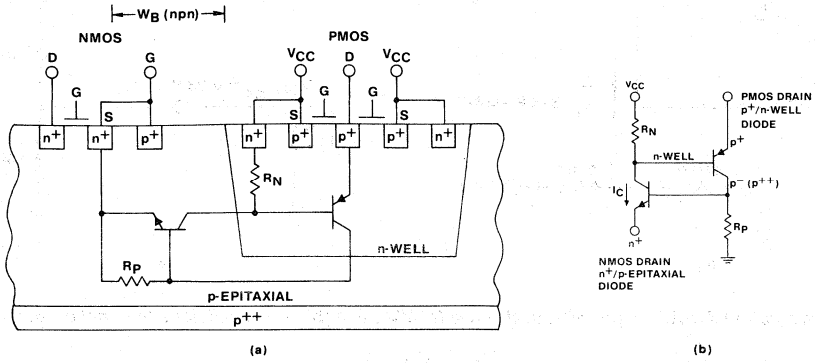


Fig. 12 - (a) Cross section of CMOS structure showing SCR latch-up parasitic transistor, (b) Simplified diagram of CMOS four-layer diode structure.

OUTPUT CHARACTERISTICS

AC/ACT outputs make use of a complementary-symmetry transistor configuration that is different from the FAST totem-pole output. Both outputs are shown in Fig. 13. AC/ACT outputs meet the voltage-level requirements necessary to interface AC/ACT inputs and the drive and current requirements needed to interface bipolar inputs such as TTL, LS, ALS, AS, FAST, and the like.

The outputs of all AC/ACT devices have the same drive current capability and meet proposed JEDEC standard drive and current requirements. The outputs may be active (two-state) or three-state in which both the PMOS and NMOS transistors are off.

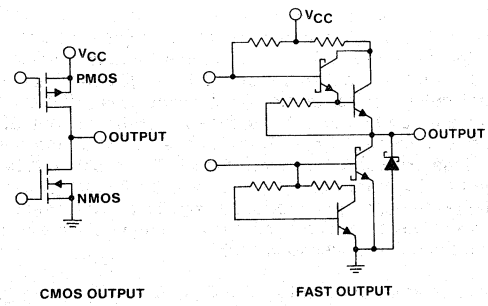


Fig. 13 - AC/ACT output, a complementary-symmetry transistor configuration, compared with FAST output, a totem-pole configuration.

Another type of AC/ACT output is the open-drain output of the AC/ACT 05 Hex Inverter shown in Fig. 14. The AC/ACT 05 is the only advanced high-speed CMOS inverter type having outputs that can be used for a "wired-OR" arrangement. There is, however, a very useful group of octal transceiver types having open-drain outputs. These types are listed below.

AC/ACT 647	Octal Bus Transceiver/Register with Open Drain (Non-Inverting)
AC/ACT 649	Octal Bus Transceiver/Register with Open Drain (Inverting)
AC/ACT 653	Octal Bus Transceiver/Register, Open Drain A Side, 3-State B-Side (Inverting)
AC/ACT 654	Octal Bus Transceiver/Register, Open Drain A Side, 3-State B-Side (Non-Inverting)
AC/ACT 7623	Octal Bus Transceiver; 3-state B Side, Open Drain A Side (Non-Inverting)

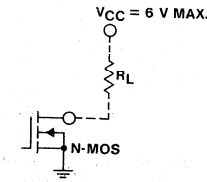


Fig. 14 - AC/ACT hex inverter (05) open-drain output circuit.

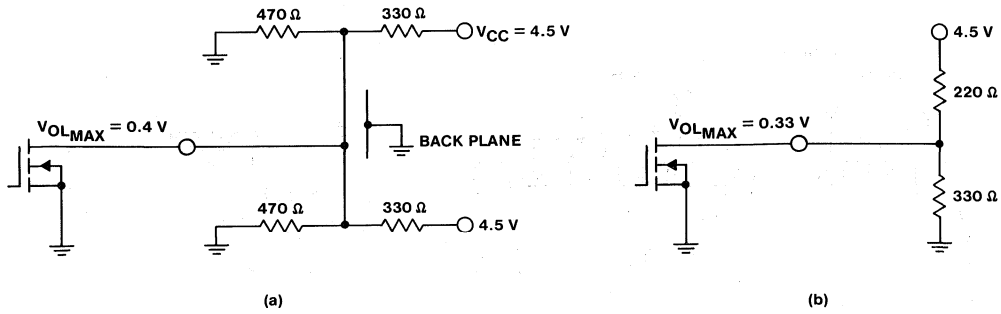


Fig. 15 - Open-drain output AC/ACT types effectively drive (a) VME and (b) SCSI backplane termination schemes.

These types are especially useful for "wired-OR"-ing of interrupt signals on a backplane. They could also be used for backplane interface using the backplane termination resistors as pull-ups. Fig. 15 illustrates two popular backplane termination schemes (VME and SCSI) that are effectively driven with AC/ACT open-drain outputs. In Fig. 15 (a), the dual VME termination scheme is driven, V_{OL} max is 0.40 volt at 85°C, and V_{CC} is 4.5 volts. In Fig. 15 (b), the SCSI termination is driven. In this network, V_{OL} max is 0.33 volt. In both examples, the bus pulls up to 2.6 volts for a V_{OH} min by means of the resistive terminations. AC/ACT types having three-state outputs may also reliably drive the VME and SCSI termination of Fig. 15. With active PMOS pull-ups, the low to high transition of the bus is faster than with the open-drain output interface. See the section on the **FCT Bus Interface Family** that describes output drives of 64 and 48 milliamperes, required in many backplane applications.

Output ESD Protection

The outputs in AC/ACT devices are protected from electrostatic discharge (ESD) damage by an integral inherent diode structure. Fig. 16 shows these diodes. These protective diodes are effective because of the large geometries (widths) of the output transistors. The diodes are comprised of the drain and the n-substrate junction of the p device and of the drain and the p-well junction of the n-device. This network provides protection to voltage levels greater than two kilovolts in all electrostatic discharge modes pertaining to the output (for these modes, see Fig. 7).

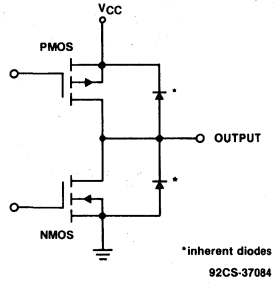


Fig. 16 - Inherent diode structure that protects AC/ACT outputs from electrostatic discharge damage to levels greater than two kilovolts.

The output clamp diode to V_{CC} must be taken into account in interface and bus applications. For more information on this subject, see the next section, **System Design.**

Output Current

AC/ACT outputs are specified for both CMOS and bipolar FAST loads. CMOS inputs are voltage sensitive, and the only current is leakage current. The output voltage test for CMOS interfacing is specified for I_O at ±50 microamperes (50 CMOS loads). The outputs are also specified for I_O at ±24 milliamperes (15 FAST loads). The corresponding V_{OL} max and V_{OH} min for the outputs are given in Table III.

For output loading of ±50 microamperes, the typical output voltage is only 60 millivolts below V_{CC} or 60 millivolts above ground. As a consequence, CMOS outputs are truly rail-to-rail swings even at 50 microamperes, which is important in many applications. The reason that the guaranteed limits of JEDEC and Table III are at 100 millivolts is to facilitate high-speed test verification.

Note that for the AC-Series types, operation down to 1.5 volts is specified. Output current is specified at 1.5 volts and also at 3 volts. This worst-case 3-volt rating is increasingly important because it corresponds to the new low-voltage logic standard (JEDEC Std. No. 8) of 3.3 ± 0.3 volts. As CMOS technology shrinks to under one micron, reliability, operating power, and most of all, switching noise all point toward more favorable results with a supply voltage of 3.3 volts than with 5-volt ones. At 3.3 volts, AC/ACT types consume only 40 per cent of the operating power of 5-volt operation, and switching speed is decreased by an average of only 30 per cent. Also, as will be covered in the section on **System Design**, TTL interface is realizable at 3.3 ± 0.3 volts using AC types.

The maximum current per output pin (I_O) is ±50 millamperes. This maximum current rating is specified when the outputs (V_O) are in their active regions, that is, greater than ±0.5 volt but less than V_{CC} plus 0.5 volt. The maximum current rating per power pin, V_{CC} or ground, is ±100 milliamperes for up to four outputs; for each additional output the rating is increased by ±25 milliamperes. When the output voltage exceeds V_{CC} by more than 500 millivolts or is below ground by more than 500 millivolts, the output protection diodes turn on and conduct current. To avoid latch-up, the peak values of the diode current I_{OK} should not exceed ±400 milliamperes, as described earlier.

An important contributor to the control of output ringing and electromagnetic interference (EMI) is an output stage design having slow enough output slew rates to allow clamp diode turn-on (about 1 nanosecond). This turn-on attenuates ringing that often tries to exceed V_{CC} +0.7 volt or go more than 0.7 volt below ground. Control of output slew rates is also a central contributor to reduced output simultaneous switching transients (discussed later).

Table III. Standard RCA and Proposed JEDEC Output Characteristics
AC Series (•For ACT Series, Specifications Only @ V_{CC} = 4.5 V and 5.5 V Apply)

CHARACTERISTIC	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		Min.	Max.	Min.	Max.	Min.	Max.	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		• -0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		• -24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	• -75	5.5	—	—	3.85	—	—	—	
	#, *	• -50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	
		0.05	3	—	0.1	—	0.1	—	0.1	
		• 0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		• 24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	• 75	5.5	—	—	—	1.65	—	—	
	#, *	• 50	5.5	—	—	—	—	—	1.65	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

NOTE: Specifications at 1.5 volts are not part of the JEDEC proposal.

Output-Current Interfacing Capability

A comparison of the output drive capabilites of AC/ACT types and FAST types follows.

FAST capability is expressed in unit loads (ULs) where the load is specified to be an input of the same family. This specification assures that the worst-case low- and high-input thresholds will be met and the existing margins of noise immunity preserved.

AC/ACT capability is expressed as source/sink current at a specified output voltage. Because AC/ACT types require virtually no input current, the unit-load concept does not apply.

With a specified output sink current drive of 24 milliamperes at 0.44 volt (at 85° C), each AC/ACT output can drive 24,000 AC/ACT inputs. With a 50-microampere/0.1-volt specification, each AC/ACT output can drive 480 AC/ACT inputs. Each AC/ACT output has a drive capability of 15 FAST loads and maintains a V_{OL} under 0.5 volt over the full temperature range.

The standardized RCA and the proposed JEDEC output characteristics are shown in Table III.

Output Curves

In Figs. 17 and 18 the standardized family output characteristic plots are provided. Both typical and worst-case (min) curves plot the I_{OL} (sink) and I_{OH} (source) current as a function of drain-to-source output transistor voltage drop (V_{DS}). The heavy line at 50 milliamperes is the boundary between safe, continuous operating regions of current drain and areas where only transients are permitted.

Output Short-Circuit Current (Backdriving)

Note that in Fig. 17 short-circuit currents of ±200 milliamperes are typical for AC/ACT outputs at a V_{CC} of five volts. Backdriving these outputs during PC board test by forcing outputs to ground, for example, is permissible with the limitations that only one output per IC be backdriven at any one time and for only one second maximum. For durations longer than one second, the IC may become too hot. Fortunately, because the epitaxial-based process is essentially latch free, no danger of latch-up results from backdriving.

Output Simultaneous Switching Transients

From Fig. 17, it is evident that very large switching transients can be absorbed by AC/ACT output transistors. Fig. 19 illustrates how large transient currents are typically generated for the charge or discharge of an AC/ACT output using a 50-picofarad load and a V_{CC} of five volts. The discharge time through the n-device of the output transistor is typically three nanoseconds, even though the capacitor discharge current is typically 83 milliamperes, as shown in the following calculation.

$$I_C = C\,(dv/dt) = 50\text{ pF}\ (5\text{ V}/3\text{ ns}) = 83\text{ mA}$$

The ON resistance of the p and n channels is 10 ohms or more each during peak switching transient periods. Thus, it is possible that switching currents of ±200 milliamperes per output may occur. For octal types, where bytes are simultaneously switched at common edges, the total peak switching current could approach 8 x 200 milliamperes or 1.6 amperes. In practice, however, the actual current is lower because it spreads somewhat as a result of the deviations in peak switching times. These currents cause device V_{CC} and ground bus voltage drops that vary with each output and hence cause different output delays. These delta delays spread the switching current over one to two nanoseconds.

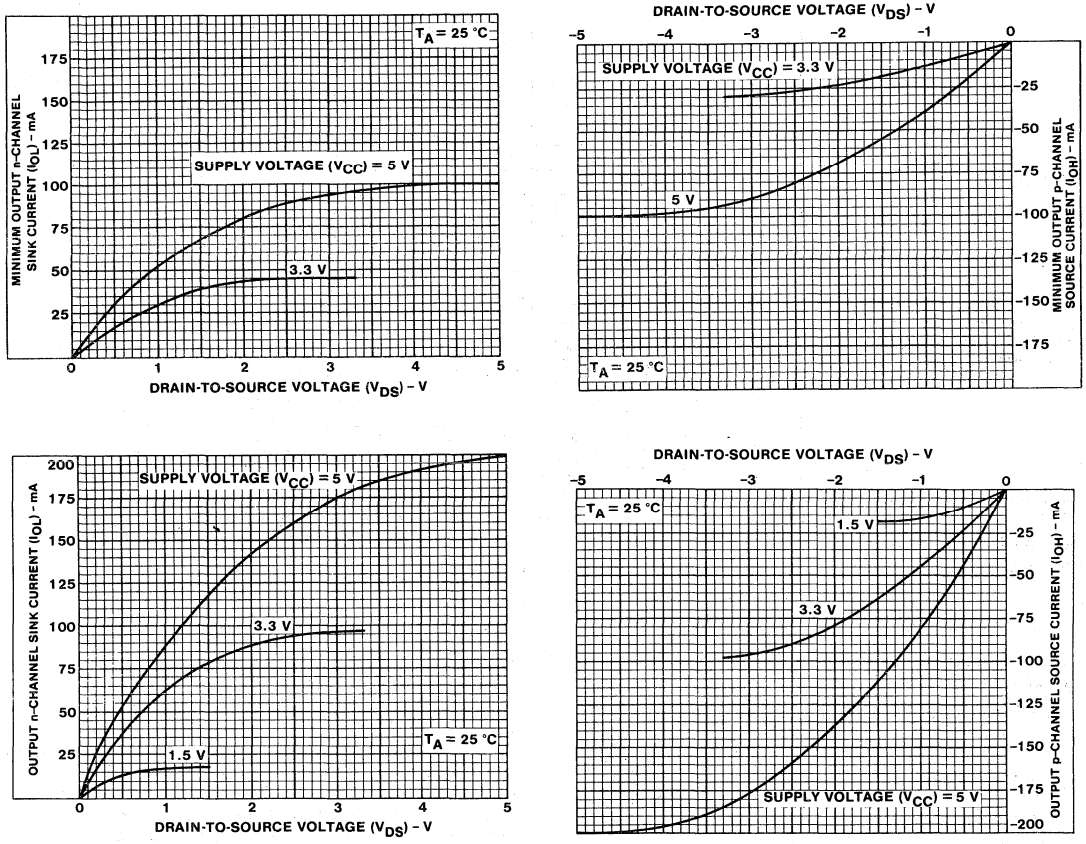


Fig. 17 - Minimum and typical output characteristics at +25° C for AC/ACT advanced high-speed CMOS types.

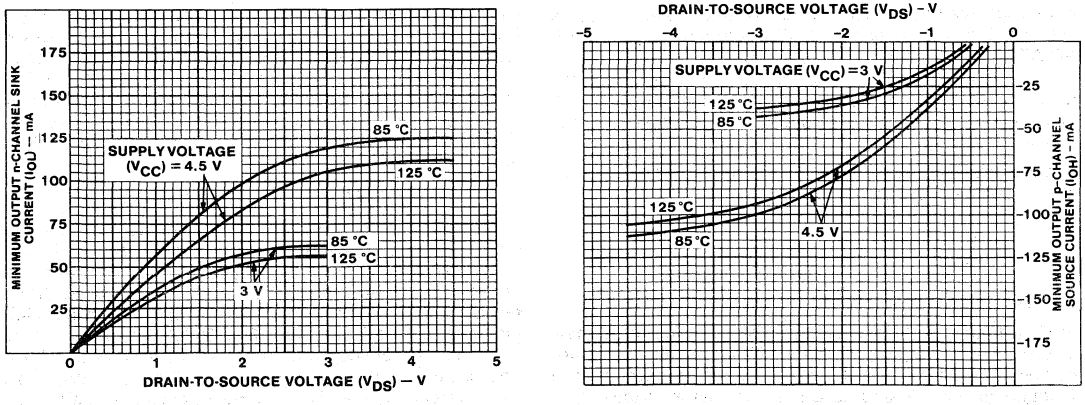


Fig. 18 - Minimum output characteristic curves at +85° C and +125° C for AC/ACT advanced high-speed CMOS types.

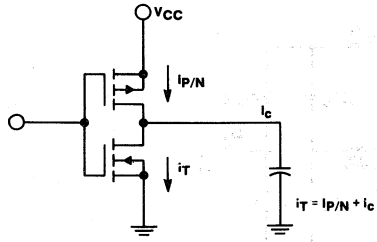


Fig. 19 - Generation of large transient currents for charge or discharge of an AC/ACT output. Load = 50 picofarads; V_{CC} = 5 volts.

Fig. 20 shows that four inductances contribute to the on-chip ground potential V_G. These inductances are L1, the effective on-chip ground path inductance; L2, the chip bond-pad/wire/lead-frame inductance; L3, the IC lead inductance; and L4, the printed-circuit board inductance path to earth or reference ground. Fig. 21 illustrates the lifting of ground as a result of the inductances L1 though L4 when an AC/ACT device switches. Instantaneously, the chip sees V_G as ground and causes the following IC performance effects.

1. If n outputs switch and one output is a steady-state low, the V_G will reflect onto the unswitched output as the peak low-level output voltage V_{OLP}, as shown in Fig. 22 (b) for an eight-output device.
2. The instantaneous gate-to-source voltage decreases by a magnitude of V_G volts. This decrease reduces the transistor g_m, raises the R_{ON}, and increases the transition time of the output stage and the delay time.
3. Input noise immunity is instantaneously decreased by V_G volts, and as a result, internally stored data in latches or flip-flops could be upset.

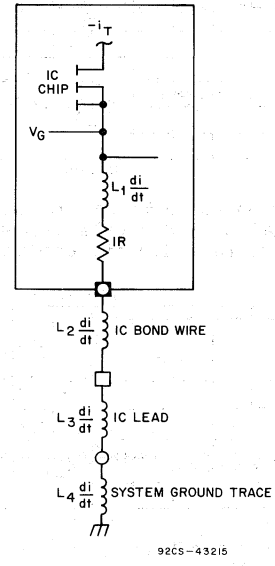


Fig. 20 - IC gound path and four contributing inductances.

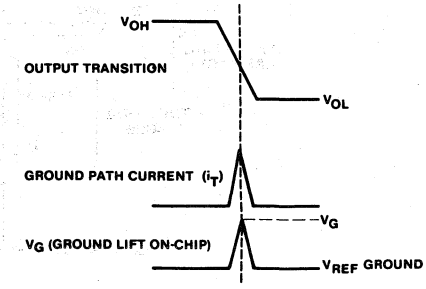


Fig. 21 - Ground lift caused by switching current transients through inductances described in Fig. 20.

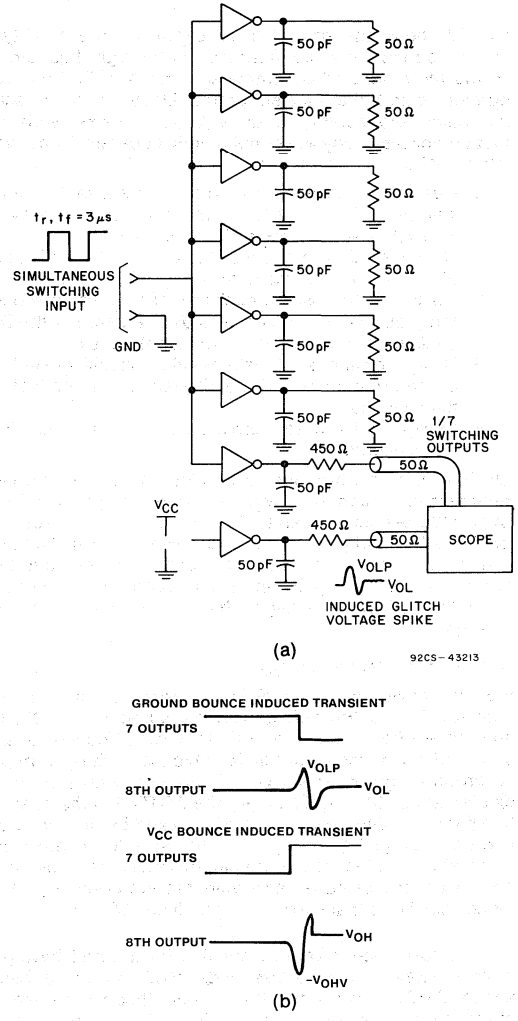


Fig. 22 - Test circuit (a) and waveform (b) of simultaneous switching transient.

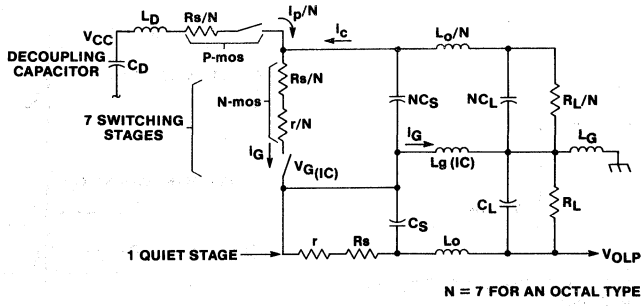


Fig. 23 - Equivalent circuit of ground-bounce configuration for an octal output stage. Dynamic value of R_S and transistor switch timing are key variables in minimizing ground bounce (V_{OLP}).

Fig. 23 shows the equivalent IC circuit for the octal-type ground-bounce test configuration. Although this circuit shows the several RLC components involved in the development of both the transient ground lift (V_G) and the resultant quiet output voltage bounce (V_{OLP}), some key variables that complicate analysis are not readily apparent. These variables include:

1. Design of transistors to increase effective R_S, which will increase turn-on time or output slew rate dv/dt. The actual value of R_S is about 15 ohms.
2. Design of chip to equalize the on-chip L and R of all eight output-stage metal runs to ground.
3. Design of the plastic package lead-frame to reduce the ground pin inductance L_g by one half. For the DIP package this inductance is 7.5 nanohenries.
4. Design of small break-before-make capability to reduce $i_{P/N}$ through current. Time difference is a nominal 0.5 nanosecond.
5. Design of transistor turn-on time of a nominal 0.75 nanosecond.

Of these five variables, the vast majority of ground-bounce minimization is achieved by control of the output dv/dt. It is of so little benefit to change the position of the ground pin or add additional ground pins that users get excellent performance and minimization of ground bounce and EMI without incurring significant extra cost and the reduced reliability of bigger packages that would result from such changes.

Sample Measurement of V_{OLP}

Fig. 24 shows actual sample measurement values of the peak low-level output voltage V_{OLP} measured on an ACT240, an Octal-Buffer Line Driver, 3-State device. The worst-case V_{OLP}, 1.06 volts, occurs at pin 18, which is furthest from pin 10 ground. The best-case V_{OLP}, 0.720 volt, occurs at pin 9, closest to pin 10. Waveforms for the ACT240 in the dual-in-line package (DIP) are given in Fig. 25 and in the small outline package (SOP) in Fig. 26. These waveforms are measured at pin 18, the worst-case pin. All RCA octals now have controlled output edge rates with ground-bounce performance similar to that shown in Figs. 25 and 26.

This performance is very reasonable for a buffer having a typical delay of 3.5 nanoseconds. RCA advanced high-speed CMOS octal logic devices have been designed to minimize the effective on-chip L1 (Fig. 20) and also to minimize L2, the dual bond-wire inductance. L3 is the inductance of a "corner-pin" dual-in-line (DIP) or small outline (SOP) package, and L4 is the inductance of the fixture ground-return path. This last value must be kept small (see next section on **V_{OLP} Measurement Method).** For comparison, a bipolar FAST F240 type was identically measured. Its V_{OLP} is nearly identical, the worst-case value being 1.05 volts.

Type: AC240
Worst-Case Value ..... 1.06 volts
Best-Case Value ..... 0.72 volt DIP
Worst-Case Value ..... 0.75 volt SOP

Type: FAST F240
Worst-Case Value ..... 1.05 volts

Fig. 24 - Measured values of V_{OLP} made on a 240 Octal-Buffer Line Driver, 3-State device.

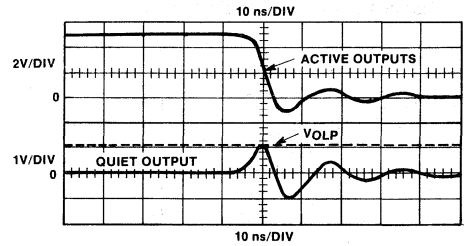


Fig. 25 - Simultaneous switching transient performance of an AC 240 octal-type IC in a dual-in-line package (DIP). See Fig. 22 for test conditions.

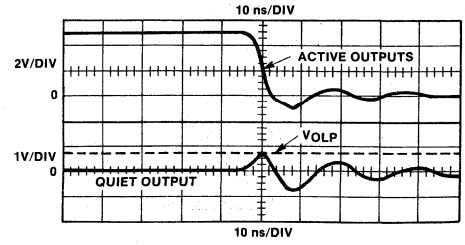


Fig. 26 - Simultaneous switching transient performance of an AC240 octal-type IC in a small-outline (SO) package. See Fig. 22 for test conditions.

V_{OLP} Measurement Method

The method for measuring V_{OLP}, also referred to as the simultaneous switching transient or ground-bounce effect, is a radio-frequency-type measurement and requires a good rf quality test fixture. A schematic of the fixture is given in Fig. 22 (a). It utilizes seven outputs switching into a standard AC/ACT load, considered to be a worst-case condition. The eighth input is held low or high, thereby placing the output in a high or low state. The eighth output is monitored with a scope, and the peak amplitude of the positive transient (V_{OLP}) above V_{OL} is measured. The peak amplitude of the negative transient below V_{OH} is V_{OHV}. Fig. 22 (b) shows the waveforms of the ground-bounce-induced transients, both positive and negative.

The major concern of the design engineer in making these measurements is the V_{OLP}. Tolerance of this unwanted noise voltage is highly dependent on the switching threshold and noise margin of the logic circuits connected to the outputs of the device. With the CMOS switching threshold, which is typically 50 per cent of V_{CC}, the energy of the transient pulse is usually insufficient to cause false switching. More critical is when the logic inputs connected to the device switch at TTL thresholds, typically 1.5 volts. See **System Design** section for a detailed examination of how simultaneous switching transients affect system noise immunity.

DYNAMIC CHARACTERISTICS

Switching Speed

Significant speed improvement distinguishes the new AC/ACT Advanced High-Speed CMOS Logic Family from the HC/HCT High-Speed CMOS Logic Family. Table IV positions each CMOS logic family with the speed-equivalent TTL family. From the standpoint of speed, the AC/ACT family substitutes very adequately for the TTL FAST, AS, and S families. It is not recommended, however, to directly substitute AC/ACT, FAST, AS, S, or ALS logic for HC/HCT or LSTTL logic because of the three times faster switching edges of the former group compared to the latter. As will be covered in the **System Design** section, these faster families require transmission-line interconnect considerations, terminations, superior decoupling, and careful PC board layout to keep switching noise generation under control so that FCC emission specifications may be met with good margin.

Table IV. Guide for Substituting CMOS Logic Family Types for TTL Families.

CMOS Logic Family	TTL Family					
	TTL	LSTTL	ALS	S	FAST	AS
HC/HCT	X	X	X#			
AC/ACT	*	*	X*	X	X	X

#HC/HCT substitutes when ALS is used versus LS for lower power.
AC/ACT substitutes when ALS is used versus LS for higher speed.
*There is too large a difference in speed and noise/EMI generation for AC/ACT to reliably substitute for TTL, LSTTL, or HC/HCT.

Propagation Delays

The useful speed of a logic family is essentially the I/O propagation delay of both low-to-high and high-to-low signal transitions from input to output.

Table V provides a comparison of AC and bipolar FAST device propagation delays for three familiar logic types; namely, a NAND gate (00), a flip-flop (74), and an octal buffer (240). Also shown is the input clock rate. For 74-series devices, the delays and also the clock rate are very nearly the same, notwithstanding that for AC types V_{CC} is 4.5 volts and T_A is 85°C and for FAST types V_{CC} is 4.75 volts and T_A is 70°C. These test conditions are clearly in favor of FAST by about five per cent. Also evident from the data sheet extractions in Table V are the balanced delay of AC types and the unbalanced (t_{PLH} versus t_{PHL}) delay of the bipolar types.

Table V. Comparison of Switching Speed for Three 74-Series AC and FAST Logic Functions.

Product	Parameter	AC	FAST	UNIT
Two-Input NAND (00)	t_{PLH}/t_{PHL}	6.2	6/5.3	ns
Flip-Flop (74)	t_{PLH}/t_{PHL}	9	7.8/9.2	ns
	f_{max}	125	100	MHz
Buffer (240)	t_{PLH}/t_{PHL}	6.5	8/5.7	ns

Useful delay is only as good as the worst or slowest delay mode or path. For the entire AC/ACT family covering over 50 different logic functions, the speed comparison illustrated in Table V holds up within a window of plus or minus a few nanoseconds. There are, however, a few exceptions going in both directions. Where speed right up to the limit of the device capability is a critical design element, the designer should precisely use published data sheet limits for either AC/ACT or FAST types. Table VI (a) lists three ACT types in which two extra buffer stages are designed in to reduce the incremental change in I_{CC} caused by switching of the input state at 1.5 volts instead of 2.5 volts, the optimum value for CMOS devices.

As shown in Table VI (b), the six-nanosecond delay of the AC04 Hex Inverter type matches the delay of FAST types. The two extra ACT buffer stages, however, extend the delay limit to a 8.8 nanoseconds. These three SSI types are the only ones having extra ACT stages, and hence, their delay limits are a few nanoseconds slower than those of their AC or FAST counterparts.

Table VI (a). Devices Having Extra Stages for Reducing Power Consumption.

Type	Number of Logic Stages	
	AC	ACT
04/05 Hex Inverter	3	5
00 Quad Two-Input NAND	3	5
86 Quad Two-Input Exclusive-OR	4	5

Table VI (b). Propagation Delay and ΔI_{CC} Values for Hex Inverter Type 04.

Parameter	AC	ACT	FAST	Unit
t_{PLH}/t_{PHL}	6/6	8.8/8.8	6/5.3	ns
ΔI_{CC} per Input	—	0.5*	—	mA

*For three stages instead of five this value would be about three milliamperes per input.

Data sheets give a finite number of specified values of switching speed at specific test conditions. The system design engineer, however, often needs to know speed limits at other conditions. For example, the propagation delay of a 74 dual D-type flip-flop clock to Q/$\overline{Q}$ is specified as:

t_{PLH}, t_{PHL} = 9.1 ns max, V_{CC} = 4.5 V, T_A = 85°C
= 2.65 ns min, V_{CC} = 5.5 V, T_A = -40°C

There are two dichotomies: (1) The PCB V_{CC} value is fixed at a given time, probably close to 5.0 volts, and (2) the temperature is fixed at a given time, probably close to 55°C. Thus, the 9.1 to 2.65 nanosecond spread, shown above, is unrealistically large. To ease this problem, Fig. 27 is provided. Using this set of normalized delay curves, the system designer can easily narrow the MIN/MAX delay for use in estimating system timing. For the 74 dual D-type flip-flop if operation is assumed at V_{CC} = 5.0 volts, and T_A = 55°C, the MIN/MAX delay spread is narrower.

t_{PLH}, t_{PHL} = 8.3 nanoseconds MAX
= 3.6 nanoseconds MIN

Use of Fig. 27 is as follows:

1. Select the max. delay from the device data sheet for V_{CC} = 4.5 volts, T_A = +125°C. Call this value X.
2. Multiply X by the normalized multiplier fractions of X shown on the vertical axis for a given value of V_{CC} and temperature.

Each AC/ACT data sheet now contains speed limits at two temperature ranges for commercial/industrial plastic packaged product. These ranges are -40°C to +85°C and -55°C to +125°C. The latter temperature range limits are also applicable to MIL product packaged in ceramic packages. Historically, commercial TTL logic types use a limited temperature range for plastic (74 series) of 0°C to +70°C. To readily determine RCA AC/ACT speed for 0°C to +70°C operation, the following multipliers (from Fig. 27) are used:

Max. Limit = 0.855 X, T_A = 70°C, V_{CC} = 4.75 volts
Min. Limit = 0.25 X, T_A = 0°C, V_{CC} = 5.25 volts

Where X is the Max. Data Sheet limit for

T_A = +125°C, V_{CC} = 4.5 volts

Also shown in Fig. 27 is the typical curve of speed vs. temperature for V_{CC} = 5 volts. The exact value at T_A = +25°C is 0.487 X.

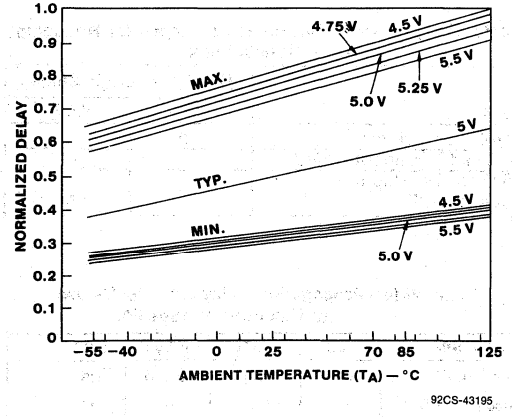


Fig. 27 - Normalized AC/ACT MIN/MAX delay as a function of supply voltage and temperature.

Propagation Delay Performance Curves

Fig. 28 shows the typical normalized propagation delay as a function of capacitance loading at supply voltages of 1.5, 3.3, and 5 volts. The reference load is 50 picofarads, the rated value given in the device data sheet. Fig. 29 shows the typical normalized propagation delay as a function of supply voltage. This curve shows that AC-Series types are typically 30 per cent slower at 3.3 volts than at the referenced 5 volts. At a supply voltage of 1.5 volts, the speed is four times slower compared to the speed at 5 volts but still is quite fast. In Fig. 30, the normalized AC/ACT propagation delay variation with chip operating ambient temperature is given for operation at 1.5, 3.3, and 5 volts. From the 5-volt curve, it can be concluded that AC/ACT types slow down by 0.3 per cent per °C, a useful number to have available for reference.

Behavioral Models

Behavior models for RCA AC/ACT types are available from Logic Automation, Inc. These models contain the min/max speed limits specified in the RCA data sheets. See section on **Behavioral Models**.

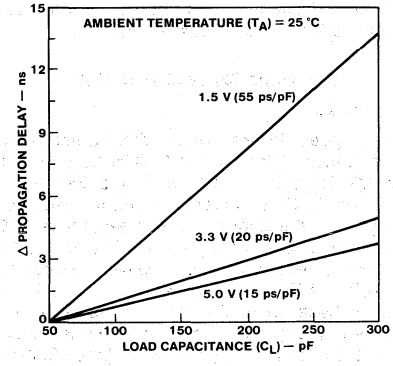


Fig. 28 - Typical change in propagation delay as a function of load capacitance for AC/ACT types.

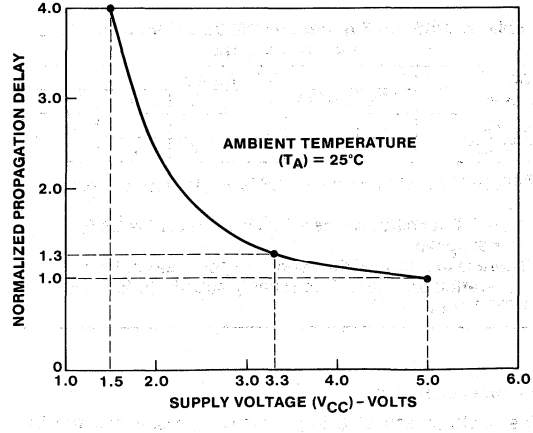


Fig. 29 - Normalized propagation delay as a function of supply voltage for AC types.

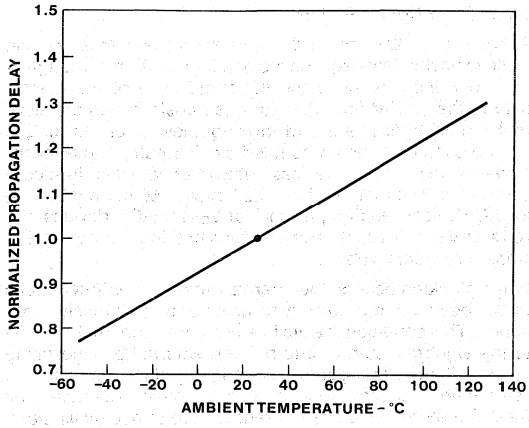


Fig. 30 - Normalized propagation delay as a function of ambient temperature for AC/ACT types.

Output Edge Rates/Transition Times

The typical propagation delay of an AC/ACT gate or buffer is 3.5 nanoseconds (at V_{CC} = 5 volts, T_A = 25°C, C_L = 50 picofarads), and the high speed of all AC/ACT types necessitates quick and predictable output transition times. Typical AC/ACT output transition times are shown in Table VII. Note that octal types have longer output transition times so as to reduce simultaneous switching transients and ringing.

Table VII. Typical Output Transition Time (t_{TLH}, t_{THL}). Measured Between the 10 and 90 Per Cent Transition Points. The ambient temperature is 25° C

C_L (pF)	V_{CC} (volts)	Typical t_{THL}, t_{TLH} (nanoseconds)	
		Logic	Octal
50	1.5	8	10
50	3.3	3	4
50	5	2.5	3.3
150	1.5	20	26
150	3.3	8	10
150	5	6	8
300	1.5	35	46
300	3.3	11	15
300	5	10	13

Fortunately, unlike bipolar FAST logic, the design engineer may insert series resistors (R_S) in the output circuit, as shown in Fig. 31, to reduce the spectral content, dampen ringing, and act as a series terminator. Propagation delay, however, will increase as a result of the series resistor and the associated total shunt capacitance C_S. For CMOS loads, an R_S, even up to several kilohms in value, will not affect input switching because the input resistance (R_I) is greater than 1000 megohms. For bipolar FAST devices, however, adding a series resistor results in increased values of V_{IL} because I_{IL} is 1.6 milliamperes. Hence, 100 ohms is probably the maximum value for R_S with FAST ICs. This topic is covered in more detail in the **System Design** section of this Manual.

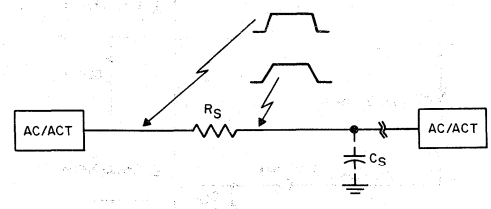


Fig. 31 - Use of series termination resistor to increase output edge rates.

Three-State Ratings and Test Conditions

AC/ACT logic types that have three-state output stage design also have the necessary three-state propagation delay parameters that are uniquely tested to optimize AC/ACT performance. Fig. 32 (a) shows an 85°C equivalent ac test circuit for all propagation delay parameters. The three "Thevininized" loads show the load board configuration for testing the six applicable delay parameters. In Fig. 32 (b) the active-to-high-impedance test waveforms are shown. Take particular notice of the RC symmetry for t_{PLZ} and t_{PHZ}, which is specially suited to CMOS rail-to-rail outputs with switching at 50 per cent of V_{CC} (AC family). Also, note that the test switch point is at 20 per cent of the rail — not 10 per cent. The reason for this increase is that 10 per cent of 4.5 volts would leave practically no room for the test set comparator because the 250-ohm load pulls rails close to 10 percent of 4.5 volts.

There are two factors that must be highlighted:

1. The t_{PHZ} test load is different from the FAST test load. For FAST, R is 500 ohms for t_{PHZ} and 250 ohms for t_{PLZ}. These test loads are very satisfactory for the bipolar totem-pole output offset to 1.5 volts for V_S and a limited swing of 3 to 4 volts, but the unbalanced loads are unsatisfactory for AC/ACT outputs.
2. FAST test points are at 10 per cent of the output swing, not 20 per cent. Because of this difference, AC/ACT t_{PHZ} and t_{PLZ} parameters are specified a few nanoseconds larger than for FAST types. This change gives the appearance that AC/ACT types are slower than FAST types, but in actual operation, they are very comparable.

Incremental Propagation Delay Caused by Simultaneous Switching

Table VIII illustrates the effects of ground and V_{CC} "bounce" resulting from the simultaneous switching of eight Octal-Buffer outputs. Note that the incremental delay added to t_{PHL} is less than that added to t_{PLH}. The reason for this difference is that the RCA chip design and the design of the bond-pad-to-lead frame are geared heavily to reducing the very critical ground loop inductance because of the 0.8-volt V_{IL} of ACT and FAST inputs. On the high side, where V_{IH} is two volts and the loaded V_{OH} is 3.8 volts, the V_{CC} bounce is not so critical. Also shown in Table VIII is the sift in skew due to V_{CC} and ground-bounce effects. The cause of these effects is described earlier in this Manual starting under the heading **Output Simultaneous Switching Transients.**

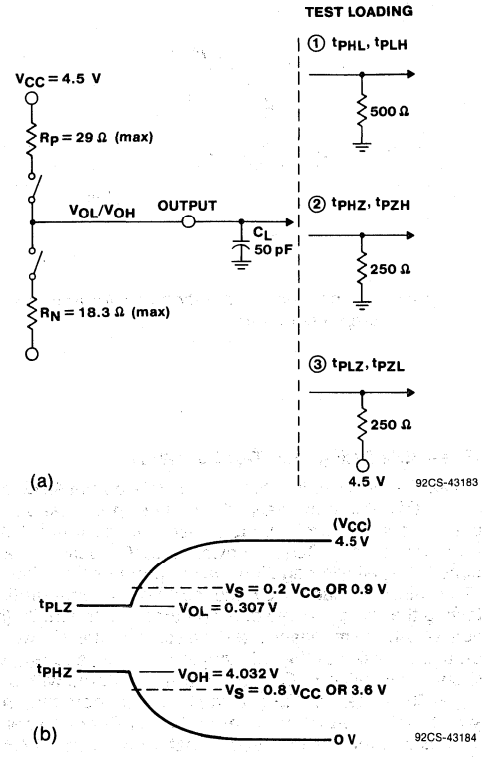


Fig. 32 - AC/ACT three-state test circuit and associated waveforms.
(a) Output stage and the three JEDEC and RCA test load circuits, T_A = 85° C.
(b) Three-state output waveforms and test points. The RC time constant is a balanced 250 ohms and 50 picofarads.

Table VIII. Incremental Propagation Delay of an AC244 Octal Non-Inverting Buffer Type.
Conditions: V_{CC} = 5 volts; C_L = 50 picofarads; T_A = 25° C.

	Number of Outputs Switching	
	1 (Best)	8 (Worst)
Buffer Measured:		
Input Pin	2	2*
Output Pin	18	18
Data (ns):		
t_{PLH}	4.9	6.41
t_{PHL}	4.88	6.04
Incremental Delay (ns) Referred To One Buffer Switching:		
t_{PLH}	0	+1.51
t_{PHL}	0	+1.16
Skew of t_{PHL}/t_{PLH} Ratio:	0.996	0.942

*Two synchronized pulse generators are used to maintain input pulse-edge integrity for precise measurement fidelity.
Generator 1 is used for driving only the measured buffer.
Generator 2 is used for driving the other buffers.

Clock Pulse Considerations

All AC/ACT flip-flops and counters contain master-slave devices having level-sensitive clock inputs. As the voltage at the clock input reaches the threshold level of the device, data in the master (input) section is transferred to the slave (output) section. The use of threshold levels for clocking is an improvement over ac-coupled clock inputs. These levels, however, make these devices somewhat sensitive to clock-edge rates. The threshold level is typically 50 per cent of V_{CC} for AC devices, and 30 per cent of V_{CC} for ACT devices (1.5 volts at V_{CC} = 5 volts). Temperature has little effect on the clock threshold levels.

When clocking occurs, the internal gates and output circuits of the device dump current to ground, as previously mentioned. This condition results in a noise transient that is equal to the algebraic sum of internal and external ground-plane noise. When a number of loaded outputs change at the same time, it is possible for the chip ground reference level (and, therefore, the clock reference level) to rise by as much as one volt. If the clock input of a positive-edge-triggered device is at or near its threshold during a noise-transient period, multiple triggering can occur. To prevent this condition, the rise and fall slew rates of the clock inputs should be limited to the maximum ratings specified on the data sheet for the AC/ACT type. The AC/ACT 14 Hex Schmitt Trigger type is recommended for sharpening up slow transitions. Under the heading **Power Consumption**, the family rating for input rise and fall time is provided, and this topic is further expanded.

Maximum permissible input-clock frequency ratings on the data sheet for each clocked device require an input clock having a 50 per cent duty cycle. At these rated frequencies, the outputs will swing rail to rail, assuming no dc load on the outputs. This feature provides a very conservative and highly reliable method of rating clock-input-frequency limits that, for the AC/ACT devices, equal or exceed the ratings for FAST types.

Low-Output Skew Flip-Flop Performance

AC/ACT flip-flop types such as the 74 dual D-type flip-flop are specially designed to have near equal delay from clock to Q and clock to $\overline{Q}$ as illustrated in Fig. 33. Dual slave sections are used to achieve this highly desirable performance. Actual delay skew between Q and $\overline{Q}$ is typically 0.05 nanosecond and a min/max spread of 0.4 nanosecond at 85° C and a supply voltage (V_{CC}) of 5 volts. Fig. 34 illustrates how this unique RCA flip-flop benefit can be used to drive a twisted pair. A termination R of about 300 ohms is desirable to match the line and reduce reflections. The key element is near-zero skew at the Q and $\overline{Q}$ output edges.

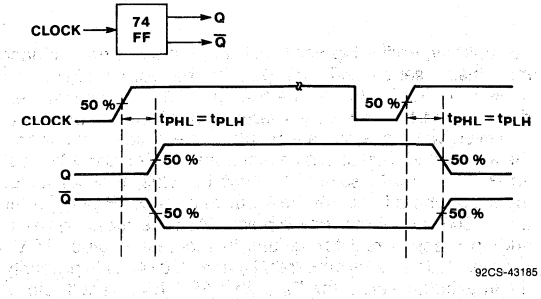


Fig. 33 - Delay balance of dual D-type flip-flop (74AC/ACT74).

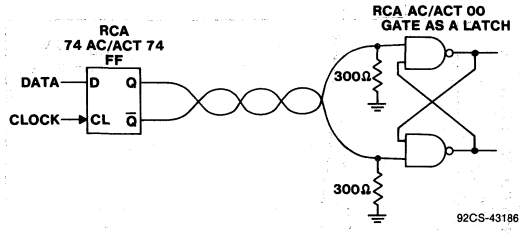


Fig. 34 - Dual D-type flip-flop (74AC/ACT74) used to drive a twisted pair.

Metastability

RCA AC/ACT clocked devices are designed to minimize the probability of output states being at an undefined or unallowable condition because of violation of Clock/Data Setup time and Hold time specifications when used in asynchronous systems. Specifically, Setup and Hold times are kept small, typically 0 to 2 nanoseconds. Also, internal flip-flop feedback paths are very fast with little delay. These design features serve to make metastability much less prevalent than for slower-speed CMOS or TTL Logic types.

POWER CONSUMPTION

The power consumption of an AC/ACT device is composed of two components: one static, the other dynamic. The static component is the result of quiescent current caused principally by reverse junction leakage. The dynamic component results from the transient currents required to charge and discharge the capacitive loads on logic elements, that is, the transients resulting from the overlapping of active p and n transistors. Internal chip power consumption is determined by the device equivalent power dissipation capacitance, C_{PD}; this parameter is defined below.

Power Calculations

Two equations are used to compute the total IC power consumption. The first equation (A) is applicable to AC or ACT devices when the inputs are driven from ground to V_{CC} (rail to rail).

Equation (A) - For AC types

$$P = P_{DC} + P_{AC}$$
$$P = I_{CC}V_{CC} + C_{PD}V_{CC}^2 f_i + \Sigma\, C_L V_{CC}^2 f_o$$

Where:

I_{CC} = Quiescent current (from data sheet ratings)
V_{CC} = Supply voltage
f_i = Input frequency
f_o = Output frequency per output
C_{PD} = Device equivalent power dissipation capacitance; used for computing internal chip power (from data sheet)
C_L = Load capacitance; used for computing output stage power

The second equation (B) is applicable only to an ACT device where specific input pins are driven at TTL levels defined as V_I = 3.4 volts for a V_{CC} max. of 5.5 volts.

Equation (B) - For ACT types

$$P = P_{DC} + P_{AC}$$
$$P = I_{CC}V_{CC} + \Sigma\, (\Delta I_{CC}V_{CC}D + C_{PD}V_{CC}^2 f_i + C_L V_{CC}^2 f_o)$$

Where:

ΔI_{CC} = Added direct current per input when $V_I = V_{CC} - 2.1$ V (TTL input high level) (from data sheet)
D = Duty cycle of clock (per cent of time high)

The temperature-dependent ratings for I_{CC} are given in Tables IX and X.

Table IX. Temperature-Dependent Rating Limits

	V_I (V)	V_{CC} (V)	25°C Typ. (mA)	25°C Max. (mA)	-40 to +85°C Max. (mA)	-55 to +125°C Max. (mA)
(ΔI_{CC})*	V_{CC}-2.1	4.5 to 5.5	0.2	2.4	2.8	3

*Additional quiescent supply current per input pin, TTL inputs high, 1 unit load
ACT load table by type shown on each data sheet.

Example: Type: ACT191; input: clock; unit load: 0.85

ΔI_{CC} = 0.85(2.4 mA) = 2.04 mA max at 25°C

Table X. Maximum Quiescent Current at V_{CC} = 5 volts for AC/ACT and FAST Types.

Device Complexity	AC/ACT Limit 25°C	AC/ACT Limit 85°C	AC/ACT Limit 125°C	FAST 125°C
SSI/FF	4 μA	40 μA	80 μA	15 mA
MSI	8 μA	80 μA	160 μA	100 mA

The dynamic power due to outputs is the sum of the ac power at each output. The user must independently determine the C_L and the average frequency of each output. The latter requires estimating the average frequency of data nodes in a logic system. For example, for AC/ACT counter types, each output is inherently operating at different frequencies.

The C_{PD}, or device equivalent-power-dissipation capacitance, is determined by two sources of internal device power consumption:

1. Power consumed by charge and discharge of the internal device capacitance.
2. Power consumed through current switching transients.

Fig. 35 illustrates the typical I_{CC} as a function of V_I for AC devices. Note in Fig. 35 (c) that when V_{IN} equals 0 to 0.5 volt or 4.5 to 5 volts, zero current flows. Thus, no ΔI_{CC} component is required for computing the power consumption of AC device types. The transient switching currents of an IC, however, consume power and are part of the C_{PD} value. The plots of I_{CC} and V_I of Fig. 35 show peak I_{CC} of up to 12 milliamperes. For a few nanoseconds, however, up to 100 milliamperes could flow if the plotter resolution permitted. Note that the switching points (peak current points) in the AC devices occur at approximately 50 per cent of V_{CC}. For the ACT devices (shown in Fig. 36) the switching point is at approximately 30 per cent of V_{CC}.

Fig. 36 illustrates the typical I_{CC} as a function of V_I for ACT devices. Again, if the input voltage equals 0 to 0.5 volt or 4.5 to 5.5 volts, no ΔI_{CC} value exists. If V_I, however, is a TTL logic high level of 2.9 volts with a V_{CC} of 5 volts, then significant ΔI_{CC} does exist (0.2 milliampere) and is indicated in equation (B) as the ΔI_{CC} component.

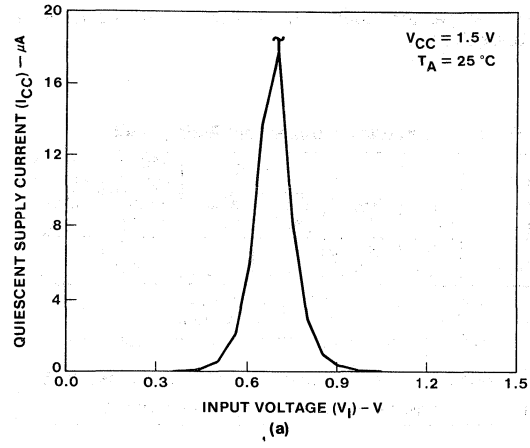


Fig. 35 - Quiescent supply current (I_{CC}) as a function of input voltage (V_I) for AC types.

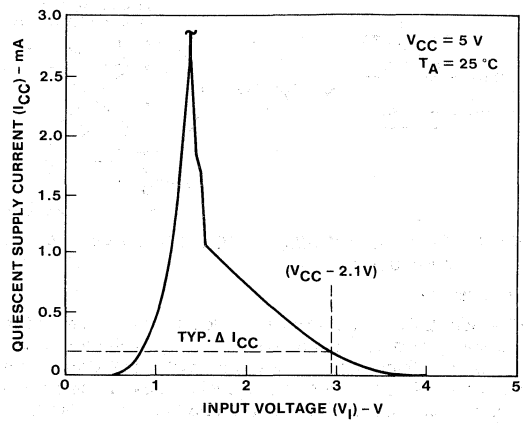


Fig. 36 - Quiescent supply current (I_{CC}) as a function of input voltage (V_I) for ACT types.

In many TTL to CMOS ACT input interface applications only CMOS loads are driven and V_{OH} is 4 volts or more. As illustrated in Fig. 36, ΔI_{CC} is 0 for TTL outputs only driving CMOS inputs. Only if a TTL output is fully loaded would the output V_{OH} be as low as 3 volts. Thus, ΔI_{CC} is usually negligible except in rare interfaces where full (15 fan out) TTL loading is present along with an ACT input.

Because the special input design of RCA ACT types reduces the value of ΔI_{CC}, the added power is small and is usually minimal compared to FAST power. If this special input circuitry were not used, the ΔI_{CC} values would be much higher.

Because appreciable current flows during device input switching, as shown in Figs. 35 and 36, it is important to maintain the fast input rise and fall times shown below.

Input Rise and Fall Slew Rate, dt/dv

	Max	Units	Inputs
at 1.5 to 3 V (AC Types)	50	ns/V	0 to V_{CC}
at 3.6 to 5.5 V (AC Types)	20	ns/V	0 to V_{CC}
at 4.5 to 5.5 V (ACT Types)	10	ns/V	0 to 3 V

Because the typical output transition time is three nanoseconds for AC/ACT types, a designer need only be concerned with exceeding the rise and fall slew rates shown above for interfacing or linear mode operation in applications such as RC oscillators, crystal oscillators, and the like.

When the Schmitt-Trigger type AC/ACT 14 is used either for shaping up slow signals or as an RC oscillator, power is increased by the prolonged through-current.

The adverse effect of power transitions is another reason to maintain input rise and fall slew rates under the recommended limits. Longer transitions may cause oscillations of logic circuits (and, hence, logic errors) or premature triggering, depending on the system V_{CC} and ground noise, which are amplified when input signals hover near the switching voltages illustrated in Figs. 35 and 36. To reduce the effects of slower transitions, the use of Schmitt-Trigger types is recommended.

Simultaneous switching transients affect the maximum input t_r, t_f. Fig. 37 illustrates a worst case but feasible condition for either a hex inverter type (04 or 05) or a hex inverting Schmitt-Trigger type (14). Using a printed circuit board designed for a ground-bounce measurement, five of six outputs are switched simultaneously causing the internal power or ground point bounce as discussed previously under the heading **Simultaneous Switching Transients.**

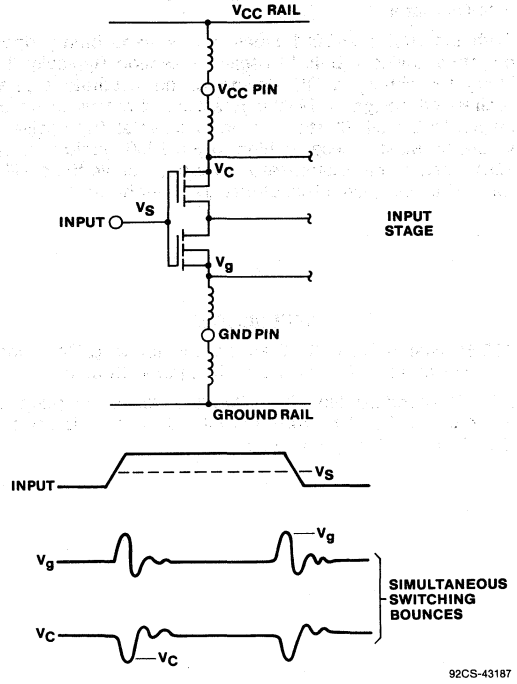


Fig. 37 - Input circuit and simultaneous switching bounces that reduce noise immunity.

Examination of the input stage and waveforms in Fig. 37 shows clearly that typical noise immunity at the input is significantly reduced during the presence of the ground or V_{CC} bounce time as quantified below:

dc noise immunity low	V_S - 0 volts =	2.5 volts (AC)
	=	1.5 volts (ACT)
ac noise immunity low	$V_S - V_G$ =	2.5 - 0.75 volts
	=	1.75 volts (AC)
	=	0.75 volt (ACT)
dc noise immunity high	$V_{CC} - V_S$ =	2.5 volts (AC)
	=	3.5 volts (ACT)
ac noise immunity high during V_{CC} bounce	$V_C - V_S$ =	1.5 volts (AC)
	=	2.5 volts (ACT)

Test results for the AC/ACT 04 and AC/ACT 14 types are illustrated in Fig. 38. The results show that the real limiting values for input t_r, t_f slew rate times must take into account simultaneous switching effects. The Schmitt-Trigger type would ordinarily be considered to have nearly infinite slew rates for one-channel-only switching. For simultaneously switching five of six outputs, there is a probably finite limitation to slew rate times. However, tests for up to 150 milliseconds per volt for AC14 and 20 nanoseconds per volt for ACT14 input slew rates (simultaneously on five inputs) did not affect the output.

V_{CC} = 5 V, T_A = 25 °C

TYPE	MAXIMUM SLEW RATES	
	MEASURED t_r	PUBLISHED t_f
AC04	>20 ns/V	20 ns/V
ACT04	>10 ns/V	10 ns/V
AC14	290 ns/V	150 ns/V
ACT14	40 ns/V	20 ns/V

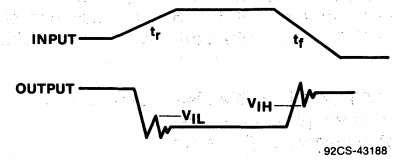


Fig. 38 - Results of typical input t_r, t_f tests on AC/ACT04/14 types. V_{CC} = 5 volts. T_A = 25° C. The maximum value of t_r, t_f is defined for condition that output ringing exceeds V_{IL} or goes below V_{IH}. Five of six outputs are switching simultaneously.

Power Consumption of FAST and AC/ACT Types Compared

As the equations for operating power indicate, CMOS power is directly proportional to switching frequency. At standby, AC/ACT power is negligible compared to bipolar FAST power. In Table XI, one of the most widely used MSI counters (the 191 4-Bit Binary Counter) is used to illustrate that even at a continuous ten-megahertz switching rate, AC/ACT power is a fraction of the power of FAST types. By way of illustration, consider an application employing 25 such types. At an overall average switching rate of ten megahertz, with FAST types the power is 7.7 watts; with AC/ACT types, the power is only 1.4 watts for AC types and 2.6 watts for ACT types.

Table XI. Average Operating Power Comparison for FAST and AC/ACT Type 191, a 4-Bit Up/Down Binary Counter. V_{CC} = 5.5 V; T_A = 70° C.

Family	Notes	Switching Rate			Units
		0 MHz	1 MHz	10 MHz	
AC	1	0.44	5.5	55	mW
ACT	2	49.4	59.9	104	mW
FAST	3	204	224	306	mW

Notes:

1. $P = P_{DC} + P_{AC}$

Where: $P_{DC} = 5.5 \times 80\ \mu A$
and $P_{AC} = 133\ pF(5.5)^2 f_i + 50\ pF(5.5)^2 + (1/2 + 1/4 + 1/8 + 1/16 + 1/16) f_o$ (Eq. A)

2. $P = P_{DC} + P_{AC}$

Where: $P_{DC} = 5.5 \times 80\ \mu A + 8 \times 2.8\ mA \times 0.8 \times 1/2 \times 5.5$ (Eq. B)
and $P_{AC} = 133\ pF(5.5)^2 f_i + 50\ pF(5.5)^2 + (1/2 + 1/4 + 1/8 + 1/16 + 1/16) f_o$ (Eq. A)

3. P = 5.5 x 55 mA (0 Hz)
P = 5.5 x 55 mA x 1.1 (1 MHz)
P = 5.5 x 55 mA x 1.5 (10 MHz)

SPECIAL RCA AC/ACT TYPES

The RCA line of AC/ACT has some unique types that are tailored for specific high-speed applications. Each is highlighted below.

CD54/74 AC/ACT7623 - Octal-Bus Transceiver, 3-State (B-Side), Open-Drain (A-Side), Non-Inverting.

The only difference from the generic bipolar type 623 is that the 7623 has an open drain on the A-side; the 623 is 3-state for both sides. The 7623 permits bus interfacing on the A-side without concern about bus contention. Also, the bus termination resistance is used to pull up the bus to a high state.

CD54/74 ACT7651 - Octal-Bus Transceiver/Register, 3-State, Inverting.

This type is logically identical to the generic 651 type with the exception that the ACT 7651 type has non-standard (and non-JEDEC) ACT output drive as shown in Table XII.

Table XII. ACT 7651 Non-Standard Output Drive.
Supply Voltage (V_{CC}) = 4.5 volts
Ambient Temperature (T_A) = 70°C

	Side A	Side B
Low-Level Output Current (I_{OL}) at 0.5 volts	12 mA	24 mA
High-Level Output Current (I_{OH}) at 3.2 volts	6 mA	12 mA

The objectives of the non-standard A-side and B-side output drive are (1) to reduce output transition time sufficiently to match slower-speed bus designs (such as Nu-Bus), (2) to reduce RFI/EMI due to slower L-H transitions on both the A and B side, and (3) to reduce the H-L transition time on the A side. This device is a noise-equivalent and speed-equivalent low-power CMOS version of the high-power-consumption bipolar type ALS651.

CD54/74 AC/ACT7060/7061 - 14-Stage Binary Counter with Oscillator.

Both the 7060 and 7061 types are 14-stage binary ripple counters having a built-in oscillator section (typically 200 MHz) for either an RC design or an accurate crystal-referenced design. A Master Reset input resets all binary stages to the all-"0" state and also disables the oscillator when the Master Reset is high in the 7060 version. In the 7061 version, the Master Reset does not disable the oscillator. All 14 binary-counter outputs are brought out.

REFERENCES

JEDEC Standard No. 8, "Standard for Reduced Operating Voltages and Interface Levels for Integrated Circuits."

JEDEC Standard No. 20, "Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices" (in preparation).

3

System Design

INTERCONNECTION OF AC/ACT LOGIC DEVICES

Interconnections of AC/ACT high-speed logic devices by means of single wires, coaxial cable, stripline, ribbon cable, or twisted pair must necessarily be designed to preserve the pulse waveform. Fig. 39 illustrates the basic interconnect environment and shows the pulse waveforms for both the ideal case and the practical or actual case with AC/ACT devices. The ideal case, shown in the waveforms of Fig. 39 (b) when one AC/ACT output port is connected to an input port of another AC/ACT part, is realizable for short interconnect lengths (less than five inches) or for the case when the line is matched by the addition of a shunt termination resistance (R_T) in parallel with the input resistance (R_I), as shown in Fig. 40.

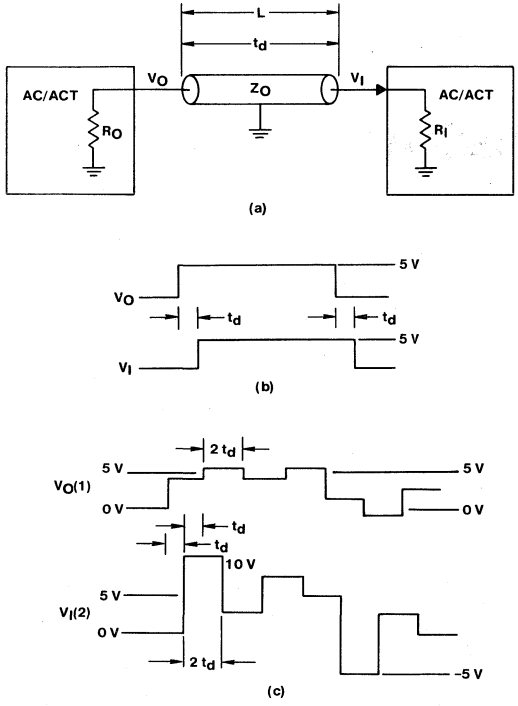


Fig. 39 - (a) Basic AC/ACT interconnect environment. (b) Waveforms for ideal situation where R_O is less than Z_O and R_I equals Z_O (matched). (c) Waveforms for actual "real-world" situation where the interconnection is unterminated, the interconnection length exceeds 5 inches, R_O is less than Z_O, and R_L is very much greater than Z_O.

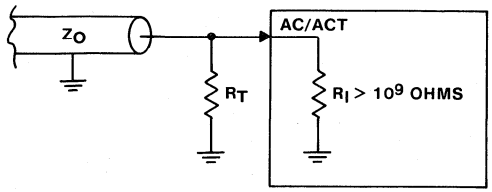


Fig. 40 - Line matched by shunt termination resistance R_T equal to Z_O. Produces waveforms of Fig. 39 (b).

If the only concern were the fidelity of the pulse waveform at the IC input or load end of the interconnection, which is often but not always the case, then a series termination scheme can be used, as shown in Fig. 41 (a). The resultant waveforms are shown in Fig. 41 (b). This figure shows a very good input pulse waveform at the load-end IC. Here, the value of the series resistor R_S is selected to make R_O plus R_I equal to Z_O. If the output resistance R_O is 25 ohms and the characteristic impedance Z_O is 100 ohms, then R_S is 75 ohms. This approach is called ideal series matching.

By studying the interconnection environment, the designer quickly learns that if the interconnection distance is "short," there is no concern and the waveforms of Fig. 39 (b) can prevail fairly well. The major design question, however, is what is "short?" Basic interconnect theory, as covered in the references given at the end of this section, states that transmission-line effects or wave effects become an important design consideration when the length of the interconnection approaches the wavelength of the signal (f_C) being transported. For AC/ACT outputs driving transmission lines, the rise time t_r and the fall time t_f can be as little as 1.5 nanoseconds. Consequently (from the theory references), printed circuit board stripline interconnect lengths of about five inches or more should be treated as transmission lines for which either series or shunt terminations may be necessary to preserve system propagation delays. Another way to state this point is that it is desired that all AC/ACT inputs switch on the first or incident pulse edge. Otherwise, a delay of $2t_d$ would be added, where t_d is the delay of the stripline (about 1.5 nanoseconds per foot).

Output Waveform and Ringing

AC/ACT outputs are inherently underdamped when driving pure capacitive loads. The industry standard ±24-milliampere balanced output drive requires an output resistance in the 10- to 20-ohm area. When applied to the RLC damping equation, this resistance value results in the underdamped condition as quantitatively defined below:

$$\text{Damping Factor } D = \frac{1}{\delta} \doteq \frac{1}{\frac{R_O}{2}\sqrt{\frac{C_O + C_L}{L_G}}}$$

Where

R_O = PMOS/NMOS device output source resistance
C_O = PMOS/NMOS device output capacitance
C_L = Load capacitance
L_G = IC ground lead inductance

If $D > 1$, RLC is underdamped
$D = 1$, RLC is critically damped
$D < 1$, RLC is overdamped

For typical values of an RCA octal buffer type with one output switching, the damping factor D is about 10 (much underdamped). This figure is obtained with the use of an R_S of 12 to 15 ohms, which is applicable to the effective output resistance for RCA octal types.

Fig. 42 (a) shows an output of a 244 non-inverting buffer with one output switching into a pure capacitive load of 15 picofarads. The underdamped overshoot is apparent. Fig. 42 (b) shows that same output switching into a pure resistive load of 100 ohms. Here, ringing is reduced because the 100-ohm resistance makes the RLC circuit nearly critically damped. Fig. 43 shows the same output driving a series 100-ohm load into 11.2 picofarads. The waveform appears like two CMOS inputs. Ringing amplitude is reduced, but the rise and fall times are about 1 - 2 nanoseconds longer. Power consumption is not increased as it is for a 100-ohm shunt load as shown in Fig. 42 (b).

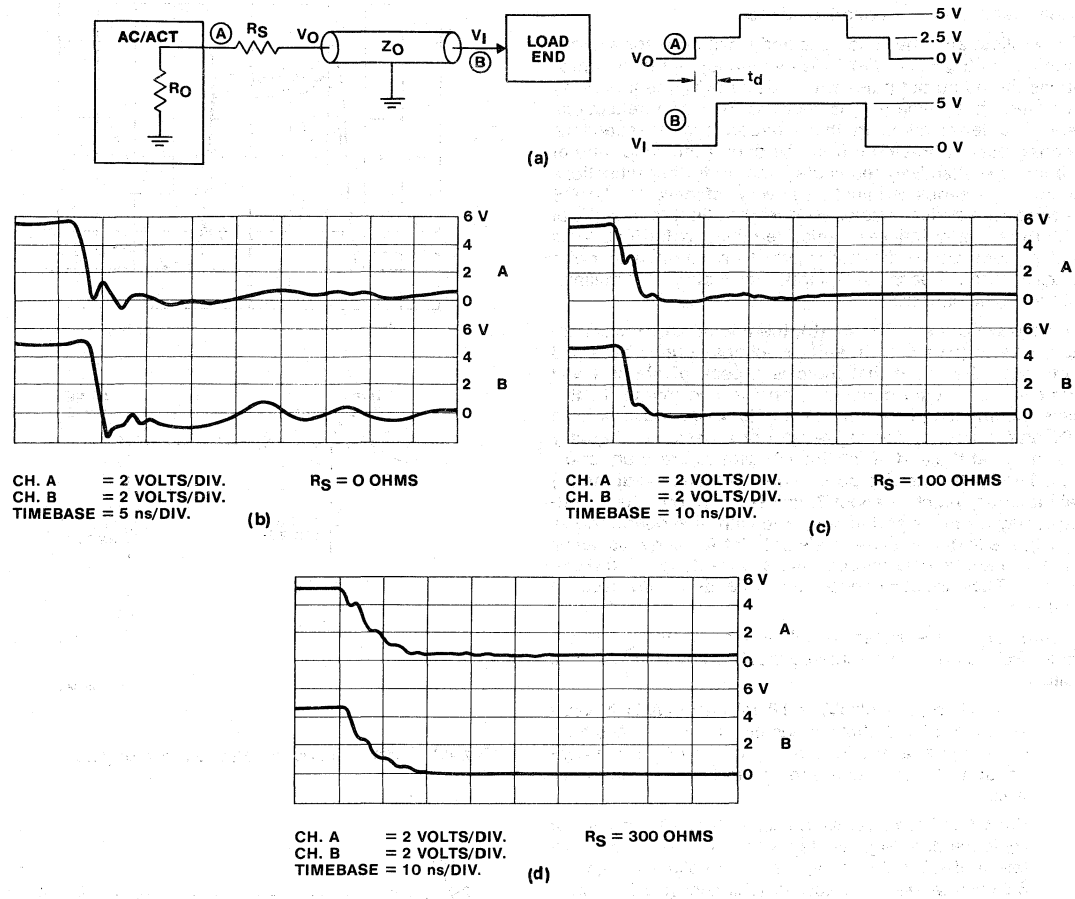


Fig. 41 - (a) Interconnect configuration showing series termination resistor (R_S) for driving from A to B through a stripline bus on a PC board. The ideal waveforms are also shown. (b) Waveforms for unmatched circuit in which there is no series termination (RS = 0) and reflections peak to 1 volt. (c) Waveforms for circuit using a 100-ohm series termination resistor (R_S). Reflections are terminated at PCB-A end. (d) Waveforms for circuit using a 300-ohm series termination resistor (R_S). Reflections cause slow signal buildup at A and B ends.

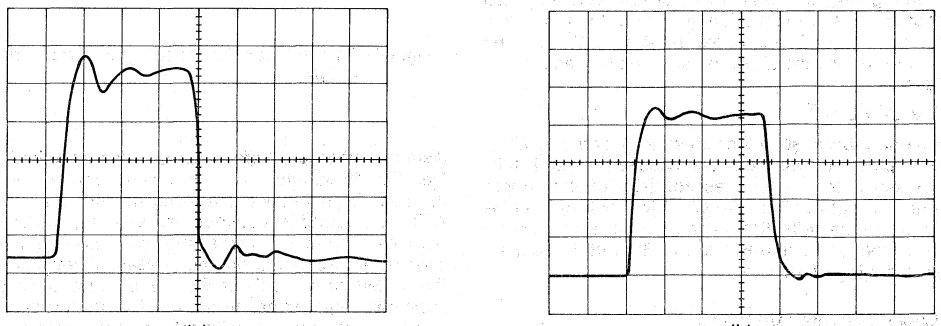


Fig. 42 - Buffer output with pure capacitive and pure resistive load makes a difference in ringing amplitude. One output switching. (a) R_L = 500 ohms; C_L = 15 picofarads (F.0 = 2 - 3) worst case. Overshoot = 0.6 volt; Undershoot = -0.4 volt (diodes help). (b) R_L = 100 ohms (driving a resistive line); good case and very often applicable.

Series Termination — Long-Line Case

Fig. 41 illustrates the schematic and waveforms for a series termination ($R_S + R_O = Z_O$). This termination faithfully reproduces the IC output pulse with a delay of t_d, the line delay over length L, where L is eight inches and reflections require a termination. In this interconnection, reflections coming back to the input from the open (unloaded) end of the line are effectively terminated and no further reflections occur. This series termination is very effective for CMOS because the series resistor R_S does not limit fanout (R_I of CMOS is nearly infinite). Series termination for TTL logic has a moderate to disastrous effect on fanout and noise margin because each FAST input draws about 1.6 milliamperes of sink current.

In the waveforms of Fig. 41 (b), there is no series termination resistor (R_S = 0 ohm) and reflections bounce back and forth with the result that there is a peak of about 1 volt somewhere in time depending on the line length. In this case the line length is 8 inches. In Fig. 41 (c) waveforms, a 100-ohm series terminating resistor provides a good quality waveform at the end of the line (B) with all areas under 0.8 volt. The fall time is also good. Note the reflection at the (A) falling edge, which is about 3 nanoseconds out, the round-trip delay for the experimental 8-inch stripline board. In Fig. 41 (d), the 300-ohm series resistor R_S at A clearly makes R_S greater than the characteristic impedance Z_o, and the waveform at B has about 5 nanoseconds of added delay because of the large R_SC_L delay.

A summary of the experimental results for an 8-inch two-sided PC board stripline interconnect of any AC/ACT type follows:

1. For TTL logic levels (V_{IL} = 0.8 volt) using ACT types, a series R_S of 100 ohms is beneficial and provides for a clean signal at the load or input end of an interconnection. A value between 50 and 100 ohms works well.
2. For CMOS logic levels, no series termination resistor R_S is needed. Signals stay within the noise immunity levels of AC logic; i.e., V_{IL}max = 1.5 volts and V_{IH}min = 3.5 volts where the typical switching level is 2.5 volts.
3. For AC/ACT devices, it is beneficial to terminate interconnections of any length to reduce the ringing amplitude, as illustrated in Fig. 43. This precaution reduces conducted EMI on the V_{CC} bus, which is always desirable.

As shown in Fig. 44, other bus drivers or receivers may also be connected to a transmission line and load the line incrementally by C_I, the distributed input capacitance. The net effect is to reduce the Z_O of the stripline bus as a result of the added C_I.

$$Z_O = [L_O/(C_O + C_I)]^{1/2}$$

Reflections occur because of the very high R_I of the AC/ACT devices at B plus the discontinuities caused by the distributed C_I. A series termination resistor (R_S) of the proper value connected right at the AC/ACT driver output pin at A effectively stops the reflection at the A end, and because there is no reflection back down to the B input, there is no undersirable ringing of the line.

Driving Cable Over Long Distances

AC/ACT types can reliably drive up to 16-megahertz data over 30 feet of ribbon cable, as illustrated in Fig. 45, where 5 megahertz is used as an illustration. The series resistor R_S (33 ohms) is used to terminate the lines. Over the 30-foot

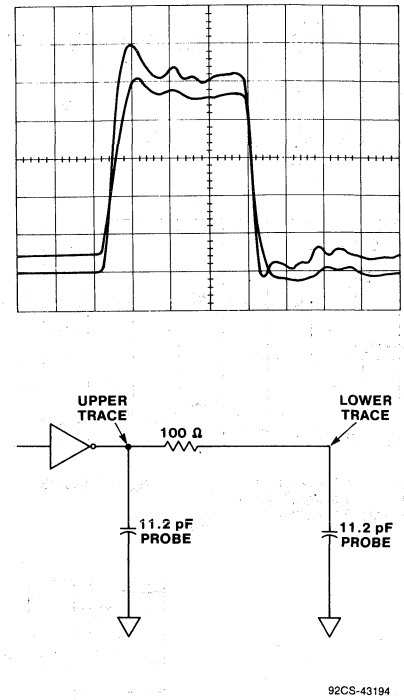


Fig. 43 - Series termination also reduces ringing.

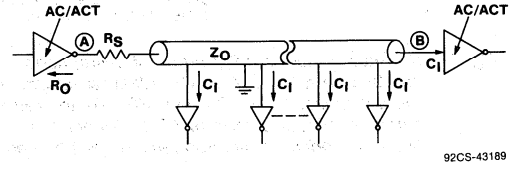


Fig. 44 - Transmission line feeding a number of AC/ACT inputs.

distance, although there is some cross coupling of signals (see Fig. 45 waveforms), it is conveniently attenuated with the small RC network at the receiving end inputs. Any AC or ACT type output is a suitable transmitting source, but only AC types should be used at the receiving end. FAST types cannot be used in this situation because they cannot handle the added series resistor R_S nor do they have the noise immunity required at the inputs. The ribbon cable recommended is No. 28 AWG with the alternate wires grounded as partial cross-coupling shields. Twisted-pair cable would be even better in this long-interconnection arrangement. Here it is recommended that the non-signal wire be grounded only at the receiving end to reduce ground-loop inductance.

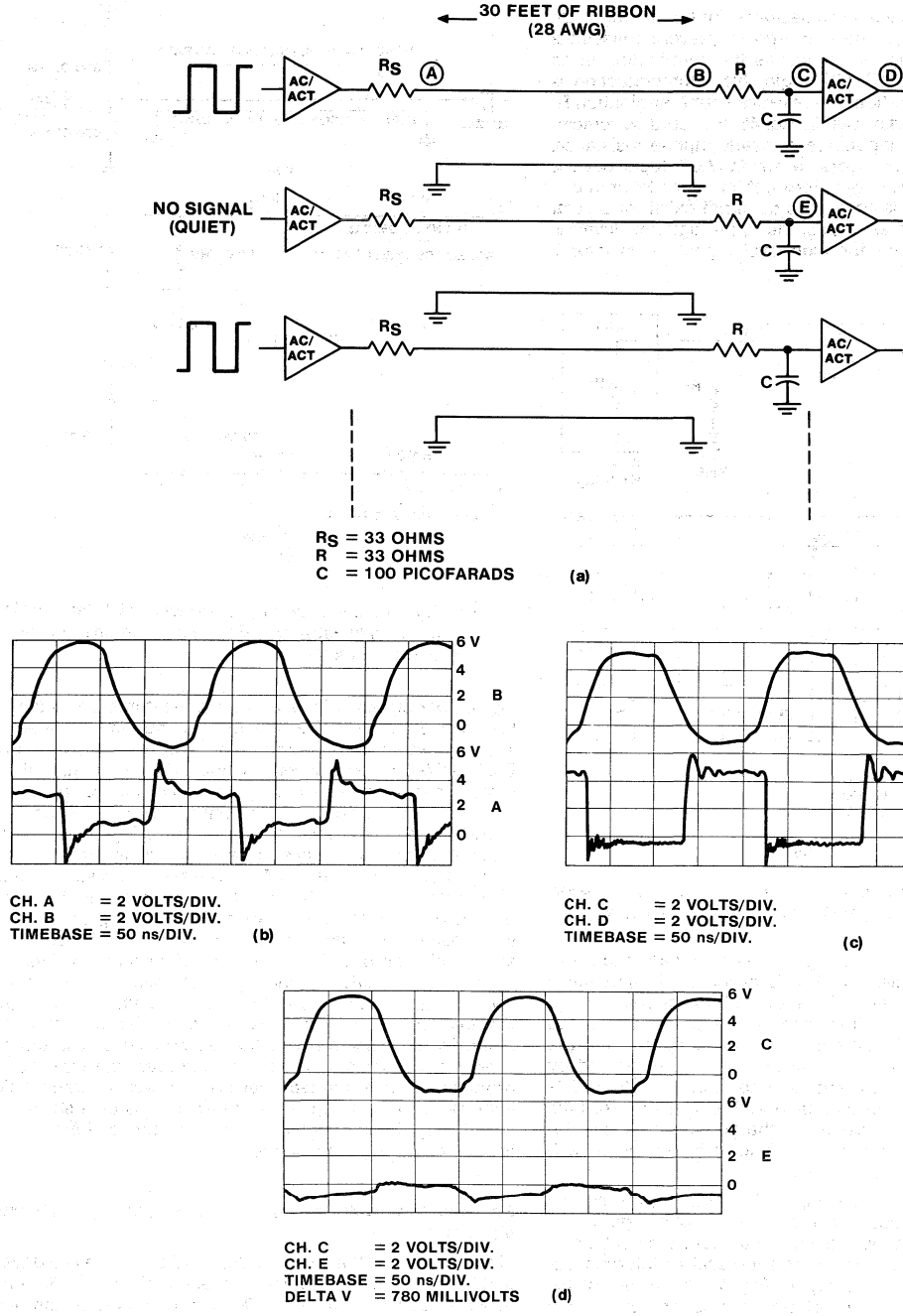


Fig. 45 - (a) Transmission of 5-megahertz signal over 30 feet of 28-gauge ribbon cable. Series termination resistor and crosstalk attenuation RC circuit are used. (b) Switched line waveforms at points A and B. (c) Switched line waveforms at points C and D. (d) Crosstalk signal on quiet line E resulting from influence of waveform at point C.

Shunt Termination — Long-Line Case

Traditional transmission lines designed for bipolar logic use shunt terminations at the load end to prevent reflections from developing. Fig. 39 (b) shows this termination in an ideal situation. For AC/ACT logic this interconnection is achieved by the insertion of a resistive shunt termination R_T right at the inputs, as shown in Fig. 46. It should be remembered that AC/ACT inputs are of nearly infinite resistance. This situation is very favorable for AC/ACT logic devices because the R_I of the device does not influence R_T or unbalance the results. This advantage does not exisit for bipolar FAST devices. For these types, the R_I for logic low levels is under 2 kilohms and for high-level signals it is over 7 kilohms.

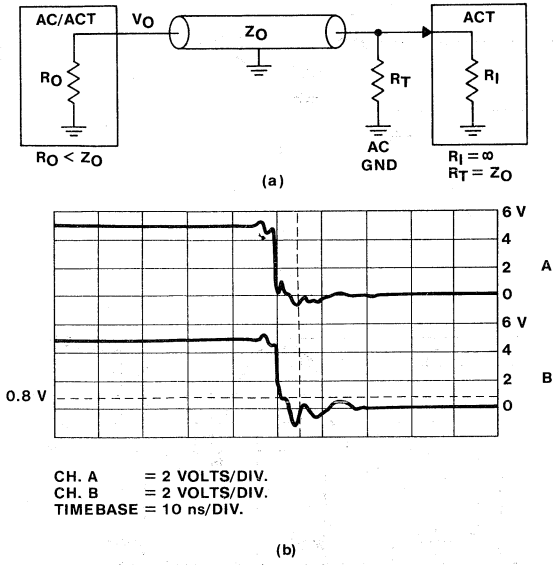


Fig. 46 - (a) AC/ACT circuit using shunt termination resistor R_T equal to Z_O. (b) Waveforms maintain integrity.

The example shown in the Fig. 47 test circuit and the waveforms in Fig. 46 (b) illustrate how excellent ACT input-signal integrity can be achieved. Note that all reflections are kept below 0.8 volt (V_{IL} of TTL and ACT types). In order to reduce the extra 40 milliwatts of power that this resistive termination generates, 11 milliwatts can be eliminated by blocking the direct current flow to ground with a 0.1-microfarad blocking capacitor in series with the 470-ohm resistor of Fig. 47. The capacitor charge time is not a factor for periodic data or clocks; it needs to be taken into consideration for non-periodic signals.

When AC types are used as input (line receiver) devices, an outstanding advantage is achieved. This advantage is that no shunt termination is required to achieve incident wave-edge switching at both ends of a transceiver interconnection, as shown in Fig. 48 (a). In Fig. 48 (b), a plot of the incident-edge signal at the drivers on either end shows that the output resistance of the AC types is low enough to attenuate reflections coming back from unterminated loads through a 50-ohm transmission line. Note that the V_{OL} of 1.65 volts and the V_{OH} of 3.85 volts meet the 30 per cent noise immunity criteria for AC types.

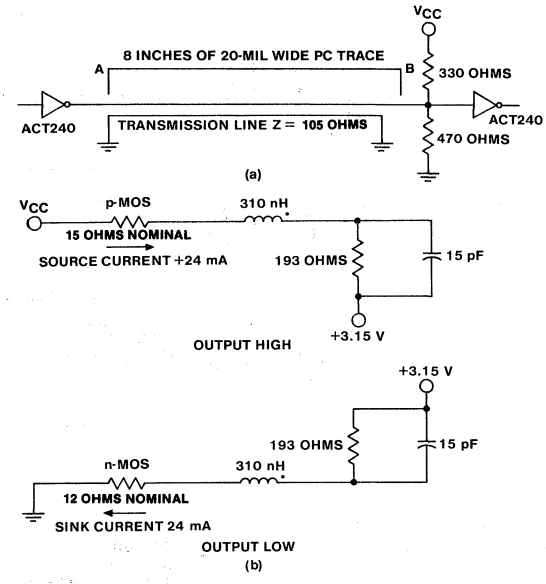


Fig. 47 - (a) Stripline interconnection with VME termination at receive end. (b) Equivalent circuits for octal device outputs.

Fig. 48 performance is valid for temperatures up to 85°C. Between 85°C and the maximum temperature value of 125°C, the transmission line Z_O must be 75 ohms or more. Each AC/ACT data sheet provides the additional high-current specification, which guarantees this performance capability; i.e., drive 50- to 75-ohm lines without power-absorbing terminations. The waveform of Fig. 48 (c) illustrates that for eight inches of two-sided board stripline, no terminations are necessary for AC types. However, for this poor type of stripline (two-sided board), the significant inductance of the PC trace causes RLC ringing that barely stays below 1.5 volts, the limiting V_{IL} for AC inputs. The simple addition of a 470-ohm shunt termination resistance to ground dampens the ringing to 1.1 volts peak, leaving a 0.4-volt noise margin. See Fig. 48 (d). With the 470-ohm termination at the input, this line could be 12 inches or more. For a transceiver type, the 470-ohm resistor would be used at both ends of the line. If a multilayer board is used to produce an interconnect having a lower characteristic impedance, the ringing would be much less than shown in Fig. 48 (c). Longer unterminated interconnections (more than eight inches) are reliable.

Simultaneous Switching Transients for Driving Transmission Lines

Fig. 49 illustrates that when an AC/ACT output device drives a 100-ohm transmission line, it really looks into a 50-ohm resistive load (two parallel 100-ohm branches of the line with Z_O = 100 ohms). The waveform of Fig. 49 shows that a peak switching transient of under 50 milliamperes is drawn for a few nanoseconds. In a worst-case situation, an octal device with eight outputs switching simultaneously could theoretically draw 8 x 50 milliamperes or 0.4 ampere.

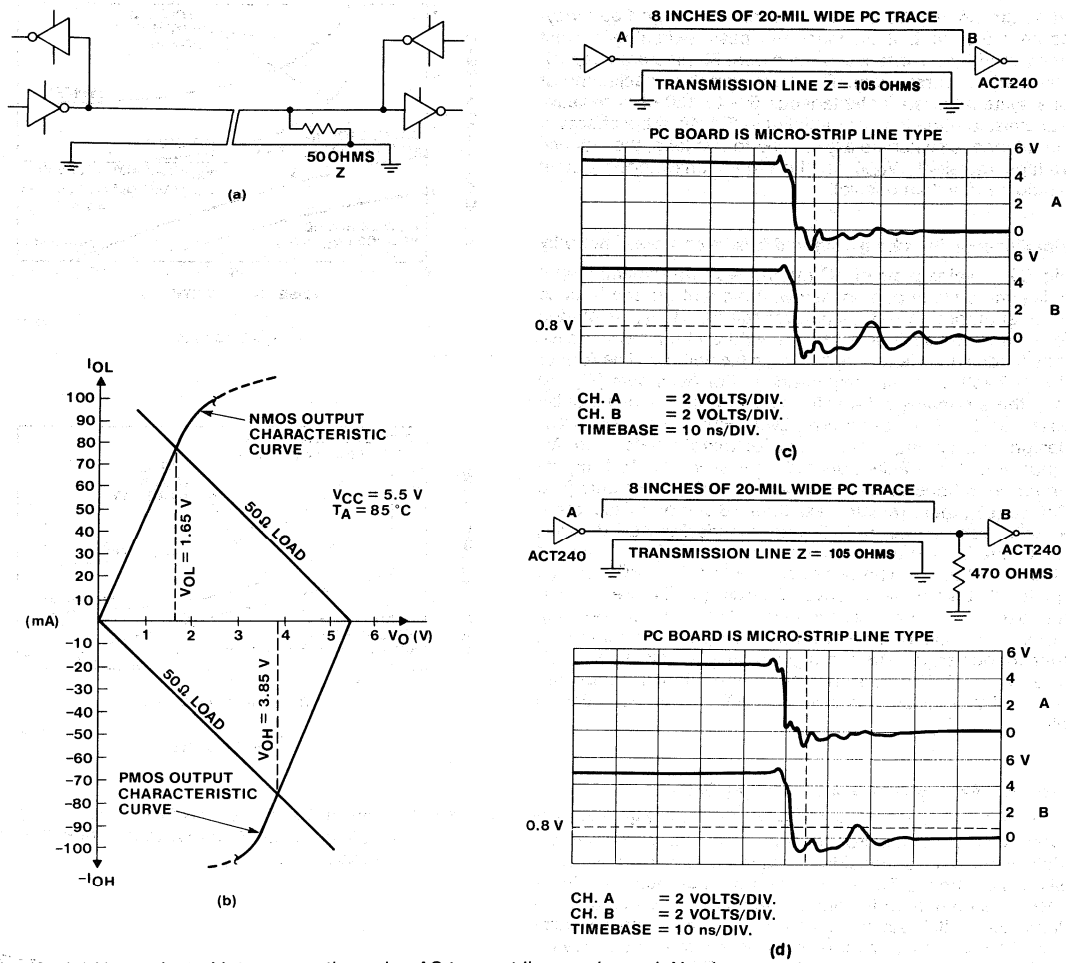


Fig. 48 - (a) Unterminated interconnection using AC types at line receive end. No shunt termination is required. (b) Plot of AC/ACT output driving 50-ohm line. (c) Waveforms for 8-inch board stripline. (d) Waveforms for 8-inch board stripline with added 470-ohm shunt termination resistance to dampen ringing.

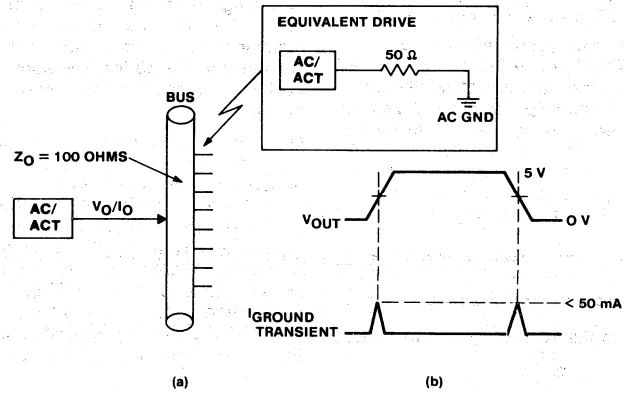


Fig. 49 - Current transient caused by line driving. (a) Circuit. (b) Waveform.

Although 0.4 ampere is a lot of current for a high-frequency-content transient, it is under the peak switching current developed by the direct drive of a pure 50-picofarad capacitive load (a worst case). The "real world" of backplane or bus systems is an instantaneous 50- to 150-ohm resistive transmission-line load as depicted in Fig. 49. If the effects of simultaneous switching are applied to this load, the induced voltage transient (V_{OLP}) on the eighth unswitched output would be less than one volt.

Simultaneous Switching Transient Effects on Noise Immunity

Fig. 50 contains plots of AC (a) and ACT (b) dynamic input noise immunity superimposed with plots of ground bounce or quiet output noise transient voltage (V_{OLP}). V_{OLP} is plotted for driving CMOS inputs (V_{OL} = 0 volt) and for a worst case fully loaded TTL fanout of 15 (V_{OL} = 0.4 volt dc). The former (V_{OL} = 0 volt) is most likely to occur. For AC inputs [Fig. 50 (a)], there remains a 1.4-volt noise margin at a noise pulse width of 6 - 7 nanoseconds. Even with rather poor PCB design and layout, there is lots of margin before an AC input would be false-triggered. However, for ACT inputs under conditions of simultaneous switching transients [see Fig. 50 (b)], there remains less than 0.6 volt of noise margin at noise pulse widths of 5 - 7 nanoseconds. For ACT designs, great care in PCB design is required to avoid false trigger of clock input loads. The designer should follow PCB design guides faithfully. Multi-Level Boards (MLB) are recommended as are terminations and optimum IC decoupling. For such a small noise margin (0.6 volt), it is recommended that trigger edge-sensitive signals such as clocks be buffered through ICs that are not compromised in noise immunity by simultaneous switching effects, as illustrated in Fig. 51.

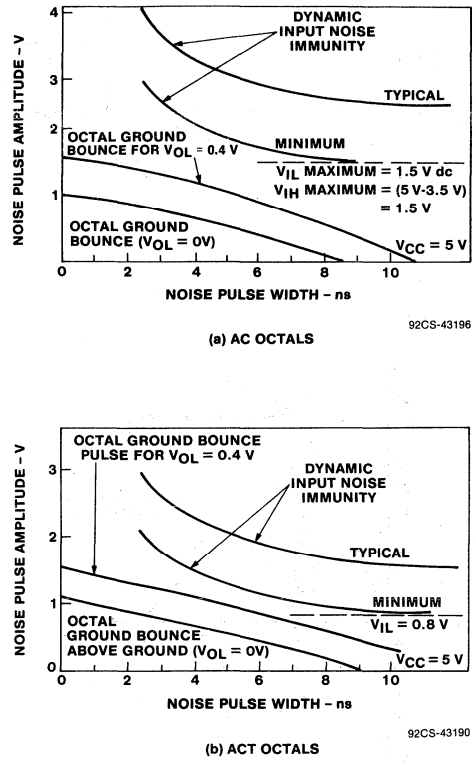


Fig. 50 - Dynamic noise immunity with superimposed plots of octal-type ground bounce to illustrate effect on noise margin.

Min/Max Propagation Delay and Delay Skew

One of the critical and system-speed-limiting parameters is worst-case min/max propagation delay. The variation in I/O delays must also consider simultaneous switching delay skew; i.e., the t_{PLH}/t_{PHL} for one output of an octal bus interface type compared to values when all eight outputs simultaneously switch. As mentioned earlier, simultaneous switching lifts the output driver ground reference and also lowers the instantaneous V_{CC} reference level. This change momentarily reduces gate-to-source voltage, reduces g_m, and produces an increase in R_{ON} in MOS transistors. Thus, the bigger the output stage RC delay, the bigger the change in t_{PLH}/t_{PHL}. See Table VIII in the **Technical Overview** section.

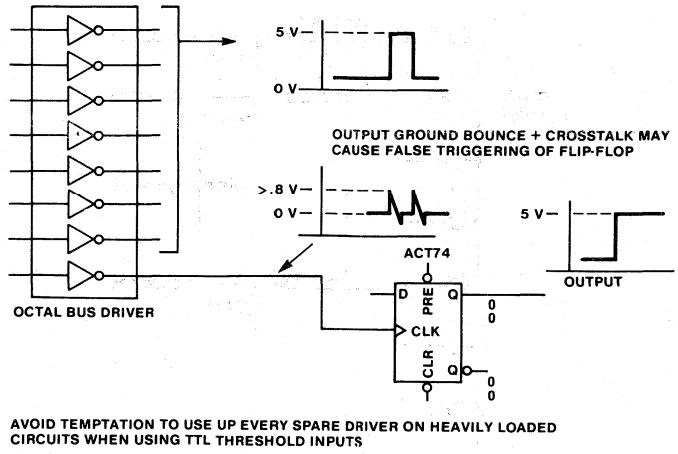
Fig. 52 illustrates some specific propagation delay skew information for the RCA ACT240 octal buffer IC. Different I/O paths inherently have a small amount of relative delay difference due primarily to on-chip V_{CC} and ground distribution — or distance to chip pads. From device layout information, five outputs have skew within a window of about 0.5 nanosecond. If only four channels are needed, pin 16 output should be dropped; then, skew is under 0.4 nanosecond because output pins 5, 7, 12, 14 have nearly identical I/O delay.

Input Terminations

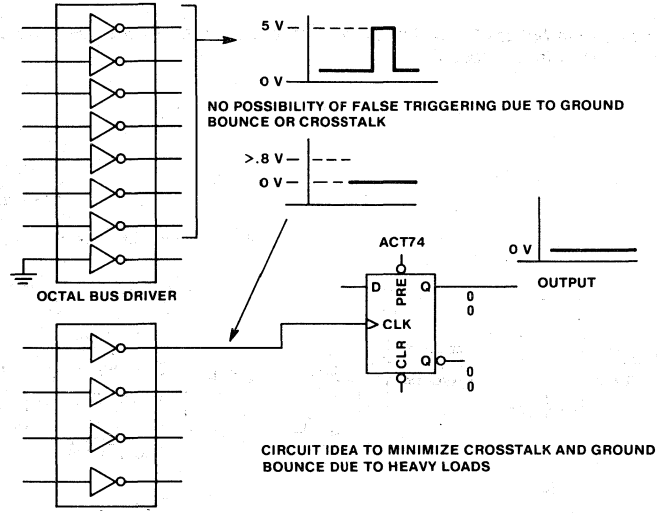
This section discusses the termination of used and unused inputs to AC/ACT devices.

Unused Inputs are terminated as shown in Fig. 53 (a). Logic inputs for non-I/O ports should be terminated to V_{CC} or ground with or without a resistor. The value of the resistor can range from 0 to 1 megohm. I/O or transceiver ports should be terminated to V_{CC} or ground only by means of a resistor of 100 ohms minimum to one megohm maximum, as shown in Fig. 53 (b). The consideration here is that if the port is in the driver mode, a short to V_{CC} or ground must be avoided.

Used Inputs are terminated as shown in Fig. 53 (c). There are application situations in which an input may become a floating one when system power is on. An example is for CMOS inputs coming off an edge card connector. If the card driving a particular bus line is pulled, then the CMOS input at the receiving PC card input becomes floating. The rule here is to terminate such inputs to V_{CC} or ground with a resistor 100 ohms to 1 megohm in value. If the interconnection is a terminated bus, however, such as a terminated VME backplane, individual input terminations such as those shown in Fig. 53 (c) are not required.



(a)



(b)

Fig. 51 - (a) When TTL threshold inputs are used, the systems designer should avoid the temptation to use every spare driver on heavily loaded circuits. (b) Circuit arrangement that minimizes crosstalk and ground bounce caused by heavy loads.

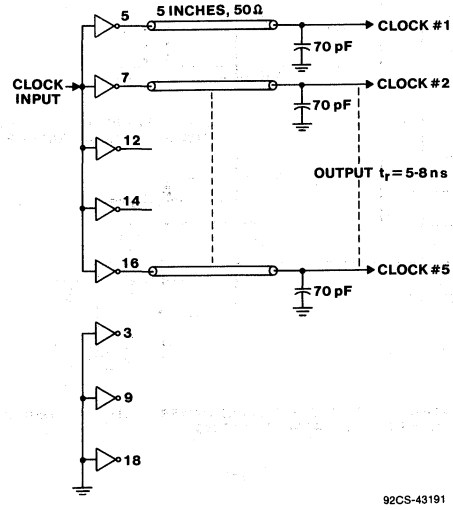


Fig. 52 - Five clock signals are buffered to within 0.5 nanoseconds skew; four may be buffered to within 0.4 nanoseconds skew if pin 16 output is not used.

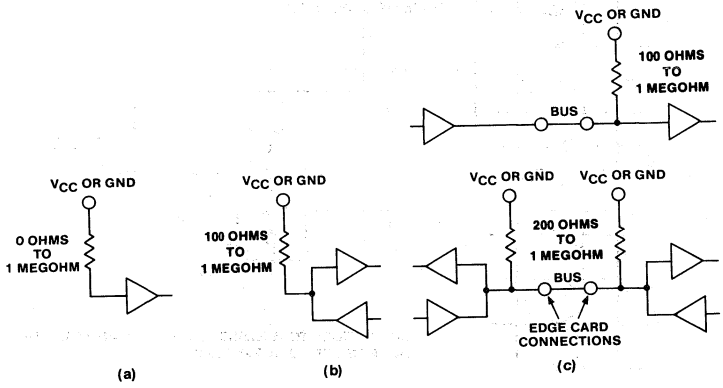


Fig. 53 - Input terminations for (a) unused logic inputs, (b) unused I/O ports inputs, and (c) used inputs coming off an edge card connector.

Insertion and Removal of Live PC Boards

"Live" insertion refers to the plugging in of a PC board or daughter card into an electrically live bus, backplane, or mother board. The designer using AC/ACT logic devices should assume that some bus activity may be electrically disrupted momentarily because of interference at plug in. Live removal merits the same considerations. Fig. 54 shows the electrical circuit for AC/ACT types that could momentarily disrupt a bus line. If either the input or output pin of an AC/ACT bus driver/receiver at the PC board interface to the bus touches the bus before V_{CC} makes contact, the entire PC board takes power off the bus line, if it is in the high state. This action would bring the V_{IH} level under the V_{IH}min value and thus the signal level on the bus would be nondeterminate until the V_{CC} pin completes contact. If a system designer requires live insertion without fault tolerance, the most reliable design solution is for PC boards to have longer pins for V_{CC} and ground. This difference in pin lengths assures that the diodes of Fig. 54 will not momentarily conduct. Because of the latch-up-free production process and circuitry, as discussed earlier, no harm to AC/ACT ICs occurs if the I/O protection diodes momentarily conduct.

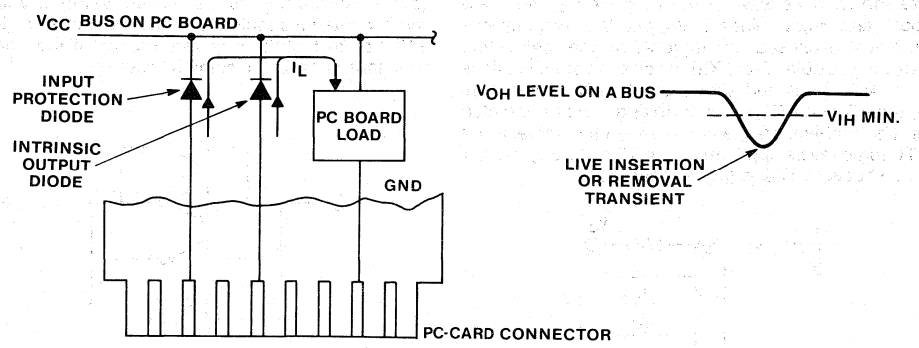


Fig. 54 - AC/ACT I/O clamp diodes can momentarily pull down a high state on a bus.

Bus Contention

When more than one driver is connected to a bus, which is usually the case as illustrated in Fig. 55, contention could occur. Considering the actual min/max spread of IC logic line delays and the differences in interconnect delays (delays are approximately 1.5 nanoseconds per foot), it is not surprising that bus contention among drivers could occur.

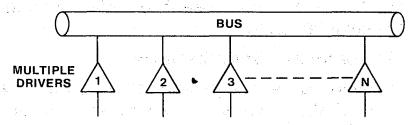


Fig. 55 - Multiple bus drivers.

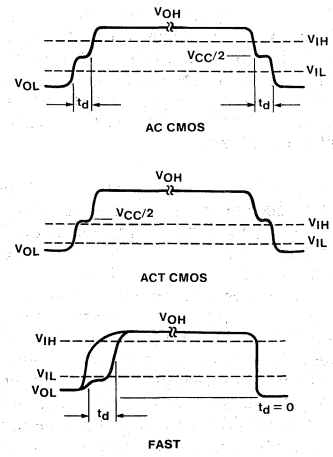


Fig. 56 - Bus contention delay waveforms for AC and ACT CMOS types and for bipolar FAST types.

Fig. 56 shows the bus contention delay waveforms for all AC/ACT 2- or 3-state output devices, except for the open-drain types. The separate waveforms for AC and ACT types are shown and compared to bipolar FAST types. Because of the well-balanced AC/ACT output drive ($I_{OL} = I_{OH}$) bus contention gives a possible mid-state delay of typically a few nanoseconds or in the worst case ($t_{max} - t_{min}$) about 7 nanoseconds. For comparison, bipolar FAST bus drivers have the same worst-case delay for the low-to-high-state changes, but the much heavier sink current (48 to 64 milliamperes) compared to source current (3 to 15 milliamperes) keeps V_{OL} below V_{IH}. Good IC decoupling is essential because, at the momentary $V_{CC}/2$ level, up to 100 milliamperes could flow from V_{CC} to ground. This condition is an example of where ACT types provide superior bus performance because of their V_{IH}min value of 2 volts.

A good solution to contention problems is the use of the AC/ACT open-drain types as bus drivers. Types suggested include the following:

AC/ACT 05	Hex Inverter with Open-Drain Outputs
AC/ACT 647/649	Octal Bus Transceiver Register With Open Drain
AC/ACT 653/654	Octal Bus Transceiver Register, Open Drain A Side, 3-State B Side
AC/ACT 7623	Octal Bus Transceiver, Open Drain A Side, 3-State B Side, Non-Inverting

With these types, not only is bus contention eliminated, but a very useful form of bus logic, called "bus wired-OR" can be used. Bus arbitration design problems are also resolved by the use of the wired-OR. Most bus designs use wired-OR for some lines, but with proper design it could be used for most or all lines so long as the pull-up delay (t_{PLH}) due to the use of resistive bus-termination networks is not excessive for the speed of the system.

Bus Drivers

Individual AC/ACT bus drivers connected to a VME bus, multibus, or other electrical backplane may have the edge waveforms shown in Fig. 57. Each bus tap has a net capacitance that ordinarily disrupts transmission line performance and produces reflections with undesirable V_{OLP} and V_{OHV}

signals, as shown in the waveforms of Fig. 57. V_{OLP} and V_{OHV} are the peak and valley values of V_{OL} and V_{OH}, respectively. If the value of V_{OLP} exceeds the logic V_{IL} or goes below V_{OL}, a logic error is possible. Table XIII reviews the specifications for AC and ACT types and shows practical values of V_{OLP} and V_{OHV} for AC and ACT outputs driving a well-populated VME bus. The problem area, emphasized in the Table, is the V_{IL} for TTL logic levels applicable to ACT or to any bipolar FAST device because V_{OLP} is greater than V_{IL}.

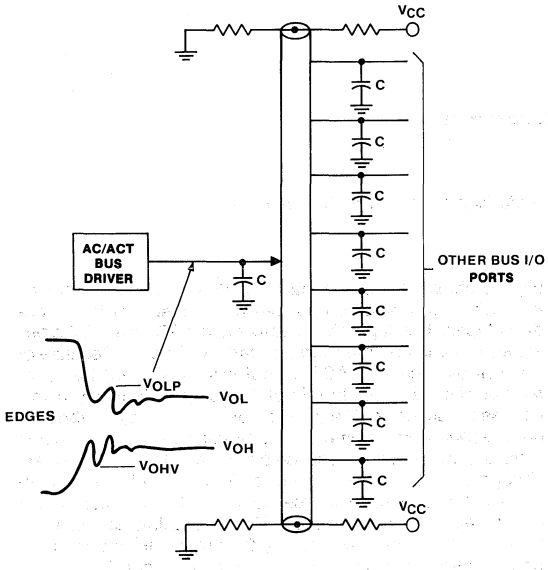


Fig. 57 - AC/ACT bus driver circuit and edge waveforms.

Table XII. V_{IL} and V_{IH} Specifications for AC/ACT Types and Practical Values of V_{OLP} and V_{OHV} for AC and ACT Outputs Driving a VME Bus.

Specifications:	AC Types	ACT Types	Units
Low-Level Input Voltage V_{IL}	1.35	0.8*	volts
High-Level Input Voltage V_{IH}	2.15	2	volts
Practical Values:			
Low-Level Output Voltage Peak Value, V_{OLP}	1		volts
High-Level Output Voltage Valley Value, V_{OHV}	4		volts

*Problem area; see text

There are several solutions to this problem. For applications of ACT types where there are data/address or non-edge-sensitive lines, the user should allow a bus settling time of 10 to 20 nanoseconds. For clocks or strobes where monotonic edges are important, the designer should increase the output device drive current by paralleling two or three (three is best but more is satisfactory) inputs and outputs of the bus interface logic functions, as shown for the AC/ACT 240 type in Fig. 58. It is very important that the paralleled functions all be in the same IC package.

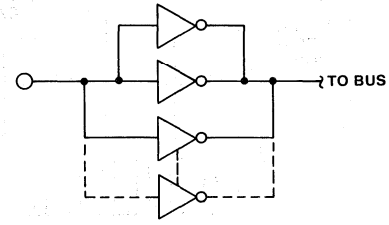


Fig. 58 - Paralleled AC/ACT functions must be in same IC package only.

For applications of AC types, this reflection problem does not exist because the superior input noise immunity of these types gives sufficient noise margin. The fastest and most reliable (compared to ACT or FAST/AS/S type applications) bus system designs are achieved with the advanced high-speed CMOS AC type ICs.

RCA FCT octal types offer an excellent solution. Outputs are tailored for worst-case backplane drive of 48 - 64 milliamperes depending on type. Output swing is two diode drops below V_{CC} to reduce switching transients. Also, the I/O diodes to V_{CC} are not present to facilitate multi-power supply system interfacing.

Multiple Power Supply Considerations

In almost every large computer system, there is a split-supply or dual V_{CC} powered situation. The power supply from one cabinet to another can have a variation of typically 10%. This figure means one IC that is driving a data bus has a V_{CC} = 5.25 volts, which is about +5%, while the receiver ICs power supply may be at 4.75 volts. With bipolar logic this difference would be of little concern, but because AC/ACT logic has built-in clamp diodes for ESD protection, a difference between power supplies could bring about greater input current flow than allowed by the maximum ratings. Figs. 5 and 16 in the **Technical Overview** section show the AC/ACT I/O clamp diodes of concern in multi-power source interconnections. This section will show two methods for dealing with the problem.

When the two V_{CC}'s vary more than 0.7 volt, current could flow from the receiver to the transmitter or from the transmitter to the receiver. If this current exceeds the ratings of the IC, the I/O current ratings could be exceeded. This condition can also hang the data bus in an undetermined state, crashing the system. Fig. 59 shows a typical example of this condition for the A --> B mode. If the difference of supplies is greater than 1 volt, the ratings of the output can be exceeded. Multiply this amount of current by 8 or more outputs, and the power ratings will be exceeded. In applications where the output current cannot be limited, the solution in Fig. 60 should be used. A low-voltage-drop diode should be placed in the V_{CC} line between its V_{CC} pin and the power supply. A 1N6263 small signal Schottky diode is low cost and has only a 0.2-volt drop. 1N914 type diodes can be used, but they have a larger voltage drop (0.7 volt). This

method of using a blocking diode provides the best solution to this problem. The ideal driver IC would not have an input pull-up protection diode or an output pull-up or pull-down diode; such outputs are present in all the AC/ACT open-drain types (AC/ACT 05/647/649/654/7623). The transmission line termination resistance connected to V_{CC} is used for the line pull-up. Bus or multiple power supply contention is eliminated. However, input diodes to V_{CC} still are present. FCT types **do not** have the I/O diodes to V_{CC}.

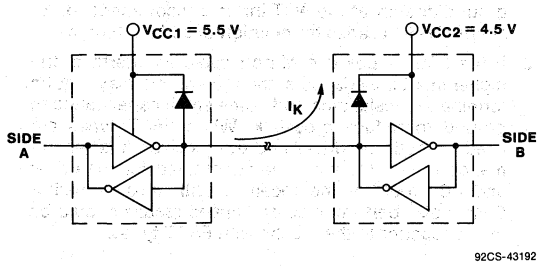


Fig. 59 - Dual power supply interface.

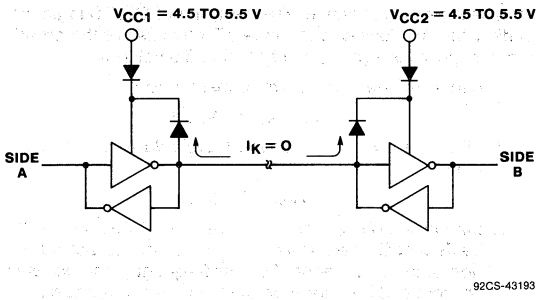


Fig. 60 - Blocking diodes in series with the V_{CC} supply pin of I/O buffers or transceivers ease multisupply interfacing.

POWER SUPPLY VOLTAGES

The GE/RCA AC types have a power supply range of 1.5 to 5.5 volts with an absolute maximum supply voltage rating of 6 volts. The ability to operate these types with a 1.5-volt supply makes them particularly useful in battery-operated equipment and especially in systems including memories that feature 1.5-volt standby operation.

The operating supply-voltage range for ACT types is 4.5 to 5.5 volts, or 5 volts ±10%. ACT types can operate down to 1.5 volts, but this mode of operation is recommended only for data retention or battery back-up.

The abolute maximum rating of 6 volts is a long-term steady-state rating for excellent reliability over the temperature range of -55°C to +125°C. A 7-volt absolute maximum rating could be met under transient conditions. The designer, however, should not deliberately operate steady state at 7 volts because of possible short-channel effects such as trapped gate charges, often referred to as the "hot electron effect." In summary, one should run the system supply or life test supply no higher than 6 volts dc even though transients to 10 volts are acceptable.

Battery Back-Up Operation

Battery back-up operation can be easily implemented in systems containing AC devices. An example of such an arrangement is given in Fig. 61. The minimum battery voltage required is only 1.5 volts plus the voltage drop of one diode. Schottky diodes should be used because of their very low voltage drop (typically 0.2 volt). In Fig. 61, GE/RCA High-to-Low Level Shifters HC4049 or HC4050 are used to prevent the flow of positive input currents into the system in the event of the input voltage levels greater than one diode voltage drop above V_{CC}. These types do not have clamp protective devices at the V_{CC} inputs. More information on this subject can be obtained from ICAN-7373, "Logic Designs for Battery-Powered or Battery-Backed-Up Operation."

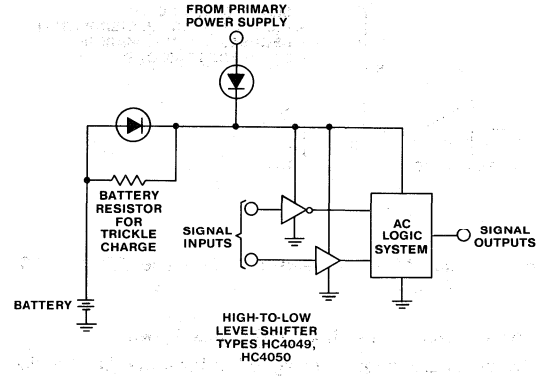


Fig. 61 - Example of AC/ACT system with battery back-up.

INTERFACING

Interfacing with AC/ACT Logic

ACT logic, like the slower HCT logic, is the most versatile logic family available for interfacing between any CMOS or TTL logic-level devices, as shown in Fig. 62. The only restrictions are the input rise and fall slew rates (see AC/ACT data sheets). If the maximum rise or fall slew rate of the CMOS or TTL output is too slow, the AC/ACT14 or HC/HC14 Hex Schmitt Trigger types are available and should be used to speed up slow output pulse edges. Note in Fig. 62 that ACT logic devices also accept NMOS logic levels.

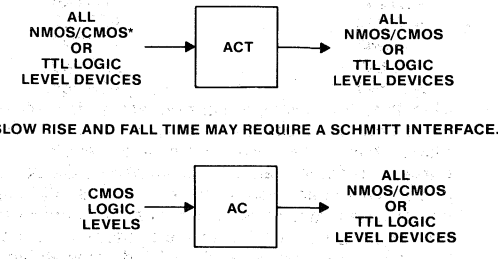


Fig. 62 - AC/ACT NMOS/CMOS interfacing using AC and ACT types.

Fanout restrictions to AC/ACT or TTL logic families are discussed in the **Technical Overview** Section of this Data Book.

AC types, as shown in Fig. 62, cannot be directly driven from any of the TTL families because the TTL output voltage high, V_{OH}min, does not satisfy the AC input voltage high, V_{IH}min, specification. To meet minimum V_{IH} requirements, AC types, however, can use a pull-up resistor, as illustrated in Fig. 63, to accept TTL logic-level inputs reliably.

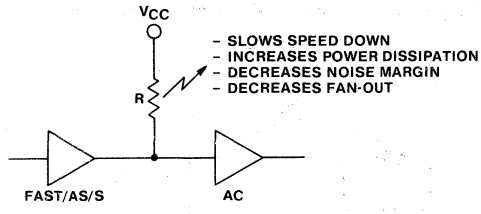


Fig. 63 - Use of pull-up resistor to interface TTL and AC devices.

Drop-In Replacements Using ACT Logic Types

ACT types are uniquely designed to have the direct logic-level interface compatibility that enables them to replace FAST/AS/S TTL logic devices of the same function as specified by the 54/74-series standard logic function nomenclature. ACT types should not be used to replace slower logic devices such as LSTTL or HCT because of the very significant three to four times faster propagation delay, edge rates, and correspondingly higher switching currents and higher EMI spectrum production. Replacement of ALS TTL devices is also a noise-generation issue, but not as severe as HC/HCT or LSTTL replacement.

There are, however, some definite possible limitations to direct drop-in replacement of FAST/AS/S types with ACT types that must be considered. The considerations are:

1. Certain bus driver types in the FAST or AS family have sink-current capabilities greater than 24 milliamperes; namely, 48 to 64 milliamperes. ACT types that are in this category include

ACT240	ACT623
ACT241	ACT646
ACT244	ACT647
ACT245	ACT648
ACT540	ACT649
ACT541	ACT654

   This 48 to 64 milliampere current value, as discussed earlier, may be necessary for driving high-fanout backplanes having resistive terminations requiring sink currents greater than 24 milliamperes. Clocks and strobe signals are also in this category, as discussed earlier (see Bus Drivers). Consequently, if power is to be saved, some redesign of the printed-circuit board is needed in order to parallel ACT devices within the same package. An excellent choice is the RCA FCT Bus Interface types for 48- to 64-milliampere sink current drivers, which are good FAST/AS replacements.

2. Trace lengths of printed-circuit board interconnections of five inches or more. A good printed-circuit-board design for FAST interconnects of relatively long length should have a shunt termination to achieve good pulse edge fidelity. Because of the high-impedance input of AC/ACT devices (R_I greater than 100 kilomegohms; C_I of 7.5 picofarads), more reflected-wave energy can occur than with FAST. Consequently, the addition of 470 ohms of termination resistance to ground directly at the ACT input is recommended. An alternative is a series termination of 50 to 100 ohms.

3. If the FAST types use ribbon cable to interface, the higher input impedance at the receive end may require termination resistance and some small capacitance to ground to reduce crosstalk. When FAST types are used for both the driver and the receiver, it is recommended that ACT types be substituted for the driver and AC types for the receiver. With these substitutions, noise performance and speed results should be much superior to the results with FAST types.

LOWER-VOLTAGE OPERATION

For CMOS logic "less is best" in terms of all-around optimum system performance. The designer of CMOS logic circuits using AC devices can make effective use of the broad-range supply-voltage capability (1.5 to 5.5 volts) to

1. Minimize operating power consumption

$$P_{operating} = CV_{CC}^2 f$$

2. Minimize switching-current transients into capacitive loads

$$I_{peak} = C\Delta v/\Delta t$$

3. Minimize EMI spectrum production. Table VII in the **Technical Overview** Section shows how output transition times and, hence, Fourier frequency components are reduced by operation at lower supply voltages.

The equipment designer can use the propagation delays as guaranteed in the data sheets at 1.5 volts or, more importantly, at the new industry standard 3.3 $\pm$ 0.3 volts (see references at end of section) to determine if the logic speed needs are being met. Fig. 29 in the **Technical Overview** Section, the curve showing normalized propagation delay as a function of supply voltage, is also very useful in this consideration.

Although these three significant benefits of operating AC logic below 5 volts, namely 3.3 volts, are enticing, there are negatives to consider besides a little slower speed. At 3.3 volts, AC logic has a speed just a bit faster than ALS TTL operating at 5 volts. These negatives are:

1. Five volts is a widely used logic supply voltage and there are many TTL and CMOS logic, microprocessor, and other devices designed for 5-volt use only.

2. Power supplies having both 5-volt and 3.3-volt taps are not currently readily available. Moreover, power supply regulation at 3.3 volts is less efficient than at 5 volts.

The design remedy for the first item above, 5-volt interfacing with TTL, is straightforward, as shown in Fig. 64. AC/ACT data sheets have full dc/ac parameters for 3.3 $\pm$0.3-volt operation and such items as sink current for TTL fanouts can easily be accessed.

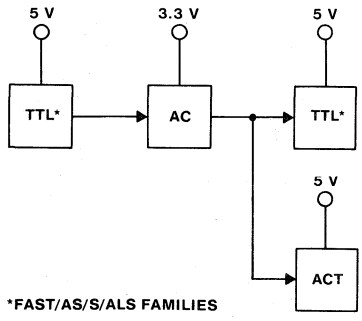


Fig. 64 - Use of both 3.3- and 5-volt supplies together.

The solution to the second item above, the lack of 3.3 ±0.3-volt regulated supplies, is not so easy to achieve. It requires design innovations through either localized 3.3-volt zener regulation from the 5-volt rail, or power supply design changes to bring out a 3.3-volt tap.

The prognosis for wider use of more optimized 3.3-volt logic or, further downstream, 2-volt logic is tied heavily into the development of even faster, smaller-geometry CMOS VLSI devices. CMOS devices with features sized at less than one micron can potentially have problems with internal electric fields that, if not remedied by process innovation, may require operation at lower than 5 volts. Also, the operating power, switching transient production, EMI generation of logic with sub-nanosecond delays point to the need for operation at lower than 5 volts. AC/ACT specifications are well poised to provide excellent 1.5- to 5-volt "glue" logic functions and data specifications as this surge to higher-speed, smaller-geometry CMOS goes forward.

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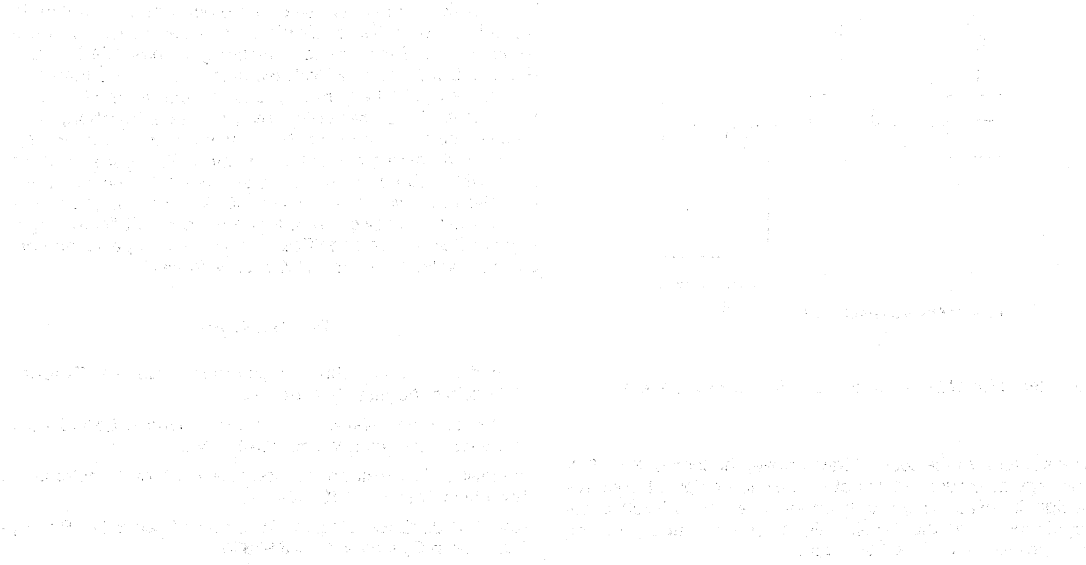
Nadolski, J. and Kalish, A., "Using Advanced CMOS Logic in a VME Data Bus System," ICAN-8640.

Nadolski, J., "Method of Measurement of Simultaneous Switching Transient," ICAN-8754.

Nadolski, J., "Logic Designs for Battery-Powered or Battery-Backed-Up Operation," ICAN-7373.



Behavioral Models

4

BOARD-LEVEL SIMULATION

In order to insure first-cut success in board-level designs, system design engineers want to be able to simulate standard IC digital products in a board-level simulation. To satisfy this requirement we teamed up with Logic Automation, Inc. to produce behavioral models for the AC/ACT product line. These behavioral models, called SmartModels® by Logic Automation, represent the RCA data sheets for each of the 130 AC/ACT types. SmartModels allow the user to simulate over a wide range of data sheet specifications, including minimum, typical, and maximum data for commercial, industrial, extended industrial, and military applications. A SmartModel is simply a behavioral algorithm that describes the function of the components and its associated timing with respect to setup, hold, maximum frequency, and propagation delay. What makes a SmartModel smart is the intelligence that the model has behind it. SmartModels try not to propagate unknown states and do not halt simulations because of timing violations. Instead, timing violations are reported on down to the precise component and pin, while the simulation continues to run with the minimum timing requirements.

ADVANTAGES OF SMARTMODELS

Before SmartModels were available to system engineers, designers analyzed board designs by bread-boarding components and methodically adding up critical path delays. Adding up the critical paths, although reasonably accurate, is time consuming and error prone. Bread boarding is a good method of proving out a final design, but it is not a good method for designing a system. Bread boarding uses a "mixed bag" of minimum, typical, and maximum products and should never be construed as verifying the manufacturability of a system.

Another method of design entails simulation with engineer-built models that incorporate the data sheet specifications. Although this method appears to be similar to the use of SmartModels, the difficulty that the system designer faces comes from the fact that models have not been verified by the IC manufacturer.

Logic Automation SmartModels for RCA standard parts are verified by GE Solid State and are tested against the data sheet. They allow the user full control of any given component in the system during the simulation of minimum, typical, and maximum products.

Example

A simple example that demonstrates the benefits of behavioral simulations is given in Fig. 65. This schematic of an AC193, a 4-bit up/down counter, excluding parallel load, has been built with the models of AC08's, AC00's, and AC74's, all Advanced CMOS standard logic products. Simulations were performed with the use of the Mentor QuickSim* simulator. Fig. 66 shows the waveforms resulting from a 20-megahertz clock pulse (up) having a 50-percent duty cycle. The resulting Q0, Q1, Q2, and Q3 output signals are counting from 0 to 15 (decimal) and upon the fifteenth count, the $\overline{TC}$ (Terminal Count Up) pulse low is generated.

® SmartModel is a trademark of Logic Automation, Inc.

*QuickSim is a trademark of Mentor Graphics Corp.

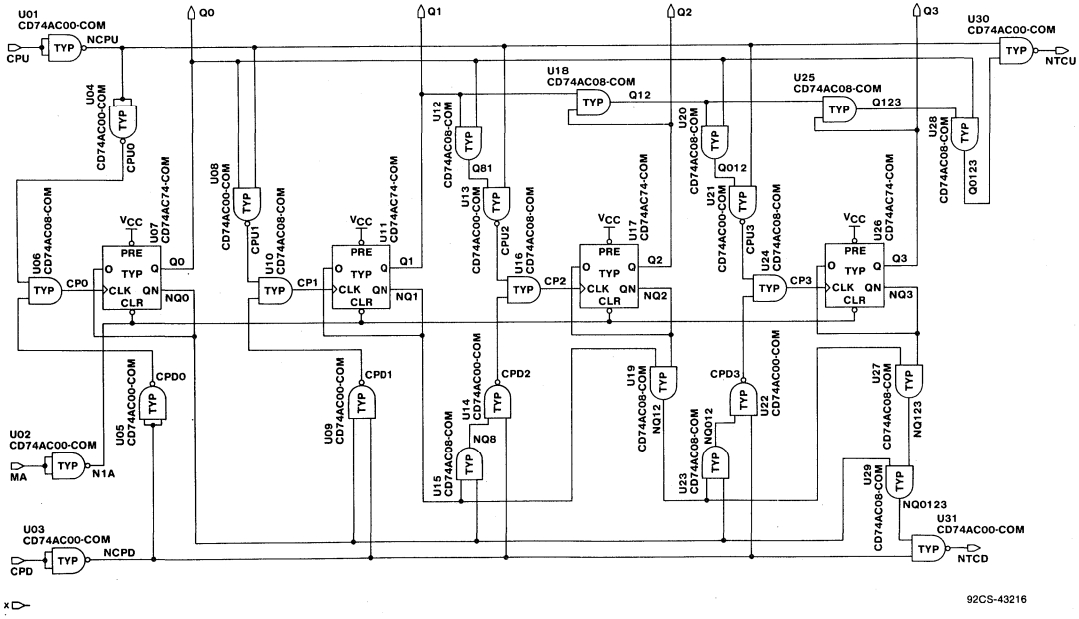


Fig. 65 - Schematic of AC193 4-bit up/down counter.

CP2 is an internal node to be discussed later. Because this counter is particularly sensitive to the clock-pulse-width high, when the pulse width is narrowed a failure should be seen as a clock pulse width that is too narrow. Table XIV shows the results of minimum, typical, and maximum simulations. The design fails at 10 nanoseconds for all models at minimum limits, at 21 nanoseconds for all models at typical, and at 30 nanoseconds for all models at maximum limits. The failing node is CP2 as displayed for a typical simulation in Fig. 67. A "glitch" due to a race condition caused by the pulse width narrowing is shown on CP2.

Table XIV - Results of Minimum, Typical, and Maximum Simulations

Minimum Pulse Width	Failure Condition
10 ns	Minimum
21 ns	Typical
30 ns	Maximum

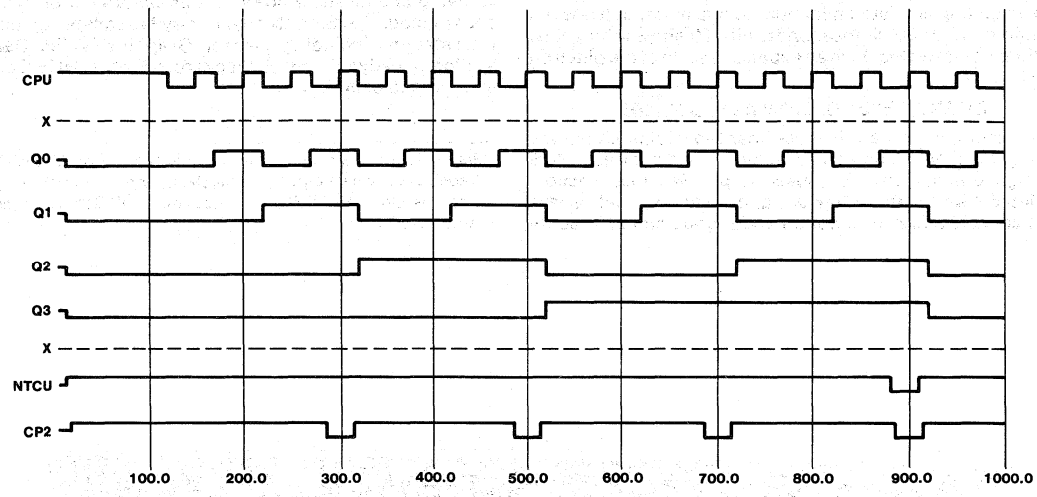


Fig. 66 - Working simulation waveforms.

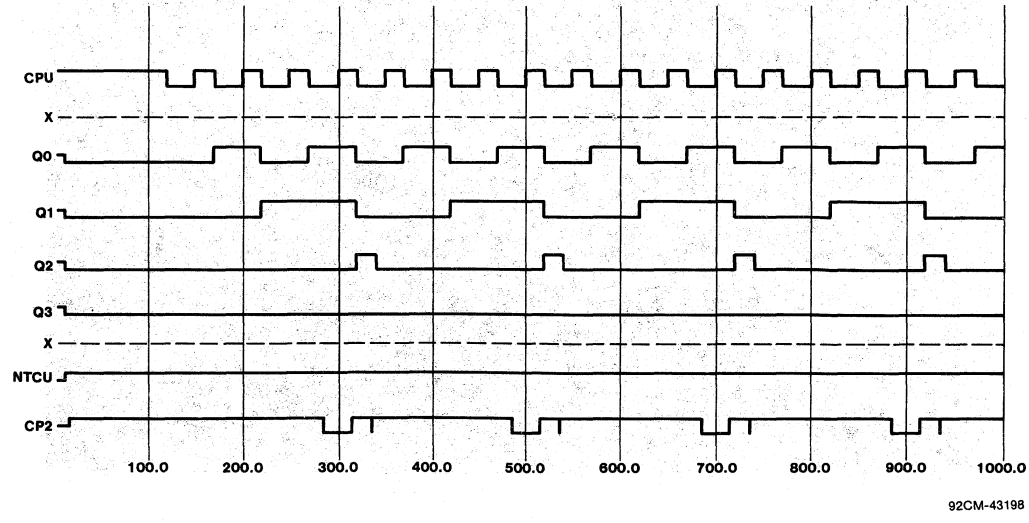


Fig. 67 - Simulation of a failure.

In order to show the validity of the simulation, a bread board was built using the same components as in the simulation. A photograph of the bread board is shown in Fig. 68. On the board an actual AC193 was included. The output of this product was gated with the mock-up of the AC193 to compare Q0 through Q3. If a difference is detected, LED's in the compare circuitry would light. The bread board has a random mix of AC/ACT product and the clock is running at 20 megahertz with a 50-percent duty cycle. Fig. 69 shows the TC waveforms of the mock-up AC193 compared to the waveforms of the actual AC193 and the waveform of the mock-up CP2 signal. When the pulse width is narrowed, the bread board fails at 14 nanoseconds. This failure result falls between the simulated minimum to maximum pulse-width range of 10 to 30 nanoseconds. Fig. 70 shows the actual failure point and Fig. 71 is an expanded scale of the glitch on CP2.

BOARD-LEVEL DESIGN ASSUMPTIONS

The assumptions made in these board-level simulations are (1) good signal integrity is achieved from proper PCB design practice for high-speed logic (See next section, **Printed-Circuit-Board Design**) and (2) analog path delays are zero. The first assumption about good signal integrity from proper PCB design is essential for any logic-level simulation. The second assumption that analog path delays are zero, although technically unachievable, is a good first-order assumption for a small PCB because the delay of interconnects is only 1.5 nanoseconds per foot. To increase the accuracy of a board-level simulation, post-layout routing extraction tools are used to determine path lengths and delays. These delays are then back-annotated into the schematic.

Logic simulation of a board design is an easy method of quickly determining design validity, but logic simulation that incorporates accurate timing is an invaluable tool for verifying and testing a board design before a prototype is constructed. The SmartModel library is available on many workstations including Mentor Graphics, Valid, Daisy, Verilog, Teradyne, Hewlett-Packard, Vantage, HHB Cadat, and more to come■.

■Mentor is a trademark of Mentor Graphics Corp. VALID is a trademark of Valid Logic Systems, DAISY is a trademark of Daisy Systems Corp. VERILOG is a trademark of Gateway Design Automation Corp.

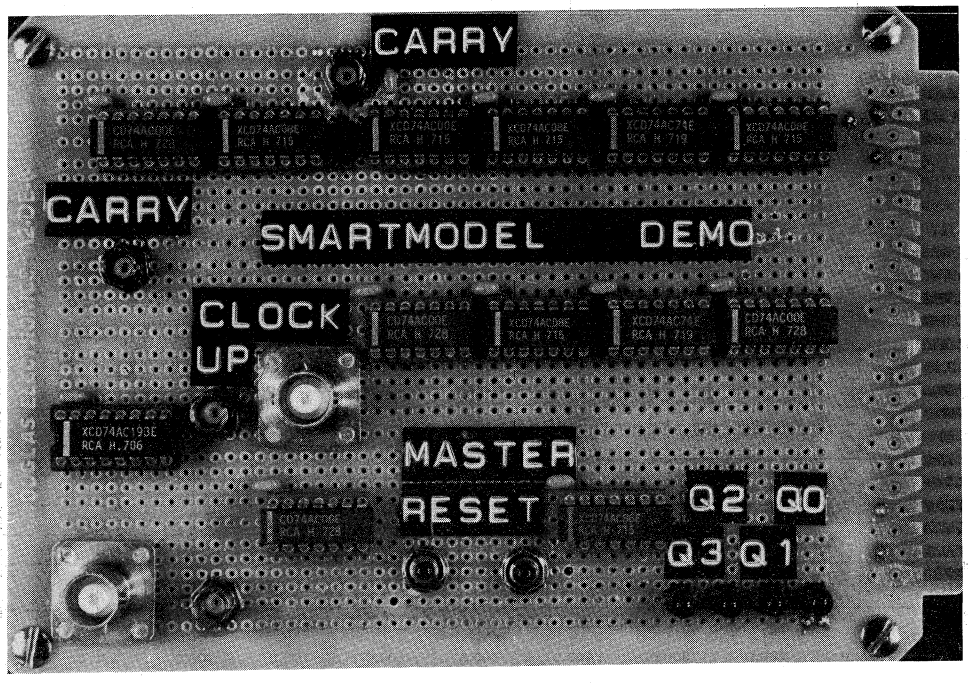
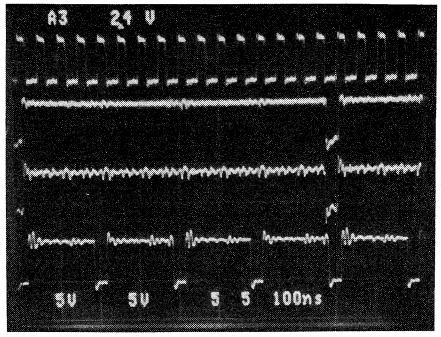


Fig. 68 - Photograph of bread board.



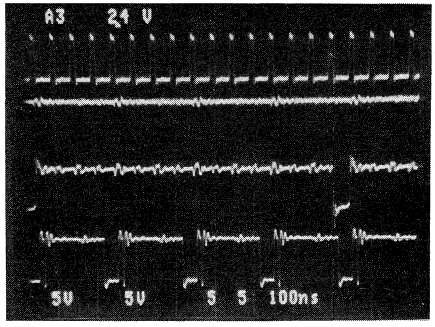
CPU Clock Pulse Up

TC Terminal Count (Mock up)

TC Terminal Count (Real AC193)

CP2 Internal Node To Q2 FF

Fig. 69 - Scope display of working circuit.



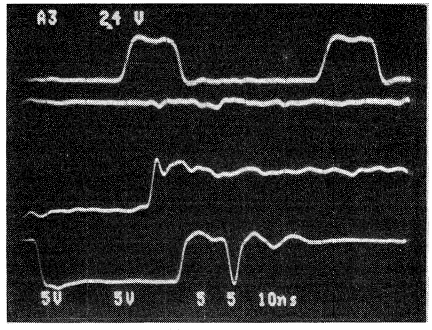
CPU Clock Pulse Up

TC Terminal Count (Mock up)

TC Terminal Count (Real AC193)

CP2 Internal Node To Q2 FF

Fig. 70 - Scope display of board failure.



CPU Clock Pulse Up

TC Terminal Count (Mock up)

TC Terminal Count (Real AC193)

CP2 Internal Node To Q2 FF

Fig. 71 - Expanded scope display of failure.

Printed-Circuit-Board Design Using AC/ACT Logic Devices

5

DESIGN GOALS

Hardware implementation of AC/ACT logic designs is largely an RF analog design issue. The system designer must follow through with critical RF electrical design techniques for printed-circuit boards (PCB) in order to achieve two goals, assuming that the worst-case logic design is complete both functionally and for MIN/MAX delay paths.

The first goal is to eliminate possible switching noise that would cause logic errors or increase propagation delay. To achieve this goal, the specific requirements are to:

a. Minimize the amplitude of the signal-line and power-line ringing.
b. Minimize reflections of relatively long (> 5 inches) interconnect paths.
c. Minimize crosstalk between signal traces.
d. Minimize the effect of simultaneous switching transients; i.e., glitching and delta propagation delay.

The second goal is to minimize power-bus ringing originating from the fast switching edges of the silicon chip. This ringing must be reduced sufficiently so that the equipment can easily pass EMI emissions standards such as the U.S. FCC class A (industrial) and class B (consumer) criteria. It is important to keep EMI from cables that would be efficient antennas at AC/ACT ringing frequencies and their harmonics.

PERFORMANCE COMPARISON

Electromagnetic Interference

A central question is "How do CMOS AC/ACT logic implementation practices compare with those of similar-speed bipolar TTL families such as FAST, AS, or S logic when it comes to the generation of low-noise PCB designs?"

The overall answer is that they are very similar in most respects in that both AC/ACT and FAST designs inherently generate considerable RF emission in the 50- to 500-megahertz spectrum. AC/ACT types, however, are a few db higher at some frequencies. There are two reasons for this difference:

1. CMOS AC/ACT outputs swing rail-to-rail or 5 volts while TTL outputs swing only 3 to 4 volts.
2. CMOS has balanced output transition times and, hence, excellent H → L and L → H propagation delay balance. FAST has relatively slower L-H transitions and unbalanced delays. This slower speed simply produces less RF spectral energy. With CMOS, because of the better balance, a part having faster speed is obtained but at the expense of a little more EMI.

From an EMI point of view, the AC/ACT family is somewhat less forgiving of sloppy PCB hardware design. This characteristic is independent of the IC ground-pin placement—center or at end of package. The EMI issue is basically specification driven.

Input Impedance

Another difference is input impedance. CMOS devices have a pure capacitive input (5-8 picofarads) and near-infinite resistance with no dc fanout restrictions. CMOS ICs, consequently, have excellent buffering capabilities. TTL devices have a 2.2-kilohm input resistance for inputs in the low state. Without suitable terminations, CMOS parts will reflect more voltage back on a transmission line.

CMOS parts, in the most desirable (AC) form with inputs switching at 50 per cent of the supply voltage, have an unsurpassed dc and ac noise margin and are three to four times more immune to noise caused by glitching, ground bounce, or interface line reflections. ACT parts suffer from the low value of the low-level input voltage (V_{IL} = 0.8 volt) of TTL parts and the resultant meager 0.3 to 0.4 volt of noise margin. Current design requirements have reached a speed for silicon logic ICs at which the V_{IL} of only 0.8 volt is a tremendous deterrent to good low-cost and super-reliable designs. New "Smart" CMOS designs using ASICs and standard CMOS logic (HC or AC form) are achieving overwhelmingly superior performance with CMOS logic levels. Those still designing at TTL levels are greatly handicapped with little margin for error in PCB design—using FAST or ACT devices.

Sensitivity to Power-Supply or Transient Variations

CMOS is further distinguished in comparison with TTL by virtue of the CMOS insensitivity to power supply dc or transient variation as shown below.

	Supply Voltage (V_{CC})	Temperature Range
FAST 74 TTL	4.75 to 5.25 volts	0 to 70°C
AC CMOS	1.5 to 6 volts	-55 to +125°C

CMOS input switching voltage points are very stable over the CMOS temperature range. TTL inputs shift four times more (0.1 volt compared to 0.4 volt). Dynamic noise immunity for CMOS is far superior over a wide temperature range.

All-in-all, CMOS AC/ACT provides for designs with superior characteristics so long as PCB layout guidelines are carefully adhered to.

PCB LOGIC LAYOUT AND DESIGN CRITERIA

This section gives detailed information on the design and layout of printed-circuit boards for high-speed logic applications. When these guidelines are followed, the designer will obtain the superior performance that CMOS AC/ACT devices can provide.

The first step is to identify "critical paths" of signal interconnections and position ICs so as to minimize the length of these paths. The guidelines are:

a. A "critical path" is any signal interconnection that is periodic such as clocks, strobes, etc. Also, any signals that drive edge-sensitive inputs such as clock inputs, resets, presets, latch-enables, etc.

b. Higher-speed logic containing "critical paths" should be isolated to a confined area of the PCB near the power entry point. This precaution reduces the inductance of the supply distribution path to high-speed logic such as AC/ACT.

c. The worst EMI generators are the periodic clock distribution chips. The higher-order clock harmonics, especially if the frequency exceeds 10 megahertz, which is likely, often are additive to the power bus ringing caused by ICs being switched. Though, special care to minimize clock-path length is beneficial, the ground return-paths for clock buffers are of utmost importance. The ground returns should be confined to a small area of the ground plane within a multilayer PCB. On two-sided boards, the ground return should be run along with the clock lines to reduce the return-path line length.

d. The best place to locate bus or backplane drivers is next to the power entry point. These drivers often drive large-value capacitors and hence generate large transients on the power buses.

PCB Material

Materials having low leakage-capacitance characteristics, such as G-10 glass epoxy or better, should be used. Lossy materials such as paper, epoxy, or phenolic are not recommended.

Multilayer Board

It is much easier to establish low impedance V_{CC} and ground returns using planes within a multilayer board (MLB) of at least four layers. V_{CC} and ground planes are buried and signal traces are on the top and bottom layers. Two-sided boards, at much lower cost, can be used effectively with proper attention to trace width and to micro-strip-line to establish trace-over-ground plane transmission lines, and the like. A ground trace can be run in parallel with the clock signals to minimize the ground-loop length and hence shorten the antenna effect.

Isolated V_{CC} and Ground Planes in a Multilayer Board

Results are usually much better in terms of power-bus EMI control if a medium- to large-size PCB has separated ground and V_{CC} plane areas for each grouping of ICs. Specific groupings to isolate noisy ICs are:

a. High-speed micros, memory, and logic.
b. Lower-speed logic and memory.
c. I/O interface circuits (near power entry).
d. Analog circuitry.

The V_{CC} and ground planes are connected by way of large independent buses to a common point (power entry point) as shown in Fig.72.

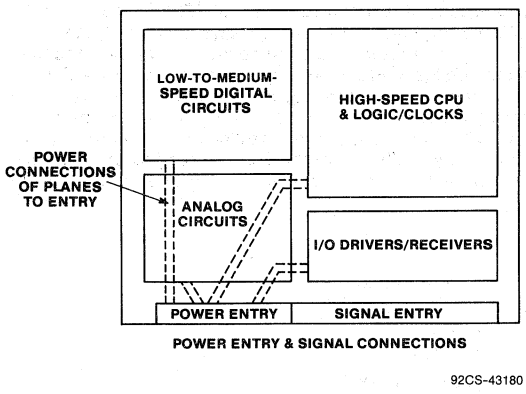


Fig. 72 - Separate V_{CC} and ground-plane areas on a multilayer PCB reduce ground-loop paths and electrical interference.

IC Decoupling

a. **Each** AC/ACT should have its own decoupling capacitor (C_D), which must be a multilayer ceramic type, or equivalent, with low equivalent series inductance (< 10 nanohenries) and low equivalent series resistance (less than 0.5 ohm). The C_D value is given by:

$$C_D = 10\ [\text{Number of outputs}]\ X\ [C_L + C_{PD}]$$

b. The lead length of the decoupling capacitor C_D to the V_{CC} and ground IC pins must be kept to an absolute minimum.
   - **Do not** decouple the V_{CC} and ground plane by tying C_D between planes near an IC.
   - **Do** connect C_D leads right at the IC V_{CC} and ground terminals. Preferred placement of the decoupling capacitor is diagonal to the V_{CC} and ground pin—under the IC or on the bottom of the PCB.
   - For SOP (surface mount), **avoid** extra inductance of through-board connections to C_D. It should be remembered that an ampere or more of high-frequency transient current courses between V_{CC}/GND pins and the C_D body.
   - The clock, strobe, etc. periodic signal generator and buffer ICs need more help than a simple C_D. They should also have a series-connected ferrite bead at the V_{CC} pin. Murata-Erie makes a three-terminal combination ferrite bead and C_D device for this purpose. The V_{CC} pin looks back to about 40 ohms at EMI frequencies of importance.

Power Bus Decoupling

Because the ringing energy from L-H transitions of a silicon chip is **the** main source of EMI, power bus decoupling both at the power entry point and throughout a medium- to large-size board is essential. Capacitance equivalent to 100 times the sum total of all C_D values on the board plus properly valued and positioned ferrite beads at power entry point makes a big difference. See Ref. 1 and 2 for more information on the decoupling design and component selection. EMI experts usually recommend distribution of many lower-value ceramic capacitors instead of a few large-value capacitors that inherently have higher equivalent series inductance and resistance.

Signal Line Traces

Following are guidelines for the design of signal-line traces. See Figs. 73 to 76.

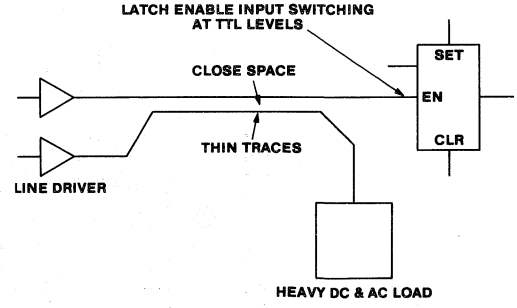


Fig. 73 - A poor layout in which high-current-driving traces are placed close to edge-triggered inputs. Crosstalk between traces can add noise.

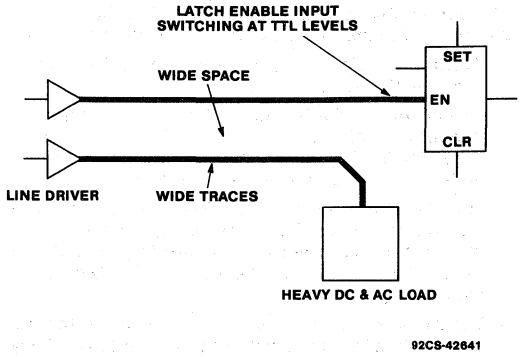


Fig. 74 - Solution to problem shown in preceding figure. Separate high-current-driving traces from edge-triggered input traces to lessen crosstalk.

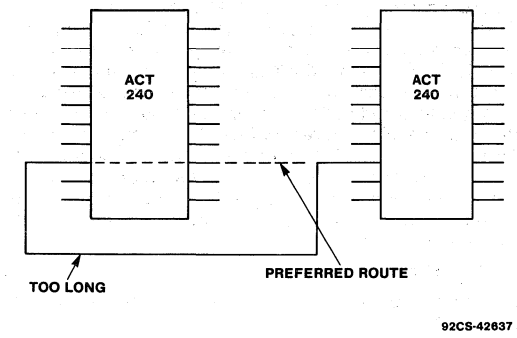


Fig. 75 - Keep interconnect lengths as short as possible. Long lengths add more inductance, and reflections are greater than with a shorter path.

a. The wider the signal line trace is the better it is because of the lower inductance.

b. The characteristic impedance of strip line or micro-strip line should be 50 ohms or higher. Values close to 50 ohms are more effective in containing EMI than higher values (greater than 100 ohms, for example).

c. Avoid 90-degree bends; use gradual bends.

d. Avoid long (greater than 5 inches) parallel runs. Long parallel runs cause crosstalk. Place a ground line between any long runs. Try to achieve 90-degree crossovers. If long parallel lines are unavoidable, attenuate crosstalk at the IC inputs with a small RC circuit (20 ohms, 100 picofarads to ground).

e. Keep paths short by using feedthroughs or vias. Line inductance is a major contribution to ringing and EMI.

Signal Line Terminations

All interconnects benefit from either a series or shunt termination for either short or long runs. There is less ringing back to the power bus and, hence, EMI is reduced.

Interconnections of five inches or more are to be strictly treated as transmission lines. For TTL logic levels either a series or shunt termination must be used. If terminations are not used, propagation delay could increase considerably because of signals not switching on incident edges. For AC logic, incident-edge switching will occur for lengths of at least 12 inches. The line resonance, however, due to the large inductance will cause more EMI than desirable. Consequently, it is best to terminate **all** traces of five inches or more. More information on both series and shunt termination is included in the **System Design** section.

Cables

As pointed out, a major factor in RFI/EMI emissions is the periodic clock signals that have high-frequency harmonics. These harmonics can be coupled into the V_{CC} bus and then to the outside world on any signal line or cable. Cables are very efficient antennas because of their length (about 1 meter) and can be the major cause of emission problems. In the PCB design, care should be taken to keep periodic clock signals physically away from I/O lines or power buses that are connected to these cables or their driving ICs. Fig. 77

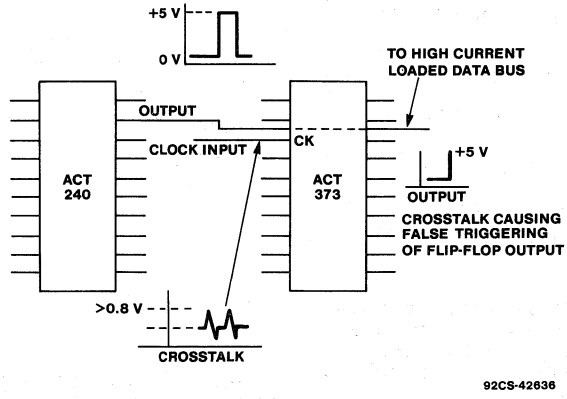


Fig. 76 - A poor layout showing a switching data bus driving a termination of 100 ohms or less. False triggering can be induced by crosstalk in this circuit. Avoid running high-current bus traces between any clock or strobe inputs.

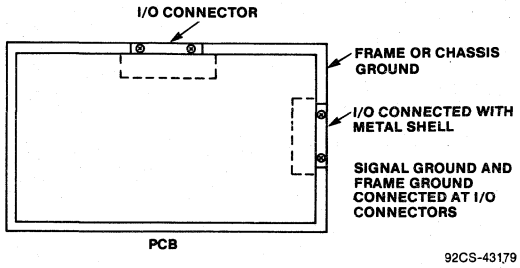


Fig. 77 - Preferred cable grounding.

illustrates a preferred method of V_{CC} and ground distribution for I/O connectors. In this example, a PCB is shown with a frame or chassis ground trace along the edge. The metal shell of these I/O connectors are physically connected to it. System ground or signal ground connects to frame ground at the connectors themselves. This arrangement creates a direct connection for any I/O grounds right back to the power supply.

Shielding

Over-reliance on equipment package or case shielding to meet FCC RFI requirements is expensive and can be a big variable. It is more economical to address power bus ringing back at the IC-PCB interface by means of the aforementioned guidelines. Some RFI, however, will be emitted by high-speed digital PCB's and some shielding is necessary. Simple metal or foil shields positioned right next to both upper and lower sides of a PCB are usually adequate—and inexpensive. With the use of simple shields, a lower-cost and RFI-leaky case can be used. Shields are grounded at the power supply outlet, on the inside of the case.

Layout CAD

At rise times of three nanoseconds and with ringing harmonics out to 500 megahertz, much manual intervention is needed to utilize computer-aided design (CAD) techniques to do an RF circuit layout properly. The goal is to build good high-speed digital interconnection and IC placement criteria into CAD. CAD, however, should not compromise the noise- and EMI-suppression guidelines needed for reliable, low-cost, equipment design. It may appear that a little time can be saved with a simple CAD program, but if the design fails to meet FCC EMI requirements, as it is likely to do without considerable manual attention from an experienced system designer, it quite possibly will have to be redesigned at added cost and lost time.

Acknowledgment—Much of the practical guidelines in PCB and equipment design to lower EMI to well under FCC limits result from the TKC, The Keenan Corporation, reference material (see references) and GESS-funded research at TKC on AC/ACT emission-reduction design techniques—which is on-going as this data book goes to press.

5

REFERENCES

R. Kenneth Keenan, "Decoupling and layout of digital printed circuits," The Keenan Corp., Pinellas Park, FL

R. Kenneth Keenan, "Digital design for interference specifications," The Keenan Corp.

FCC Emissions and Power Bus Noise - 2nd Edition, The Keenan Corp.

Reliability

MONITORING SYSTEM

The RCA AC/ACT series of Advanced CMOS Logic Integrated Circuits has an established reliability data base showing excellent reliability assurance. RCA has in place a reliability monitoring system that assures a continuation of excellent reliability by timely identification of negative trends in reliability performance so that corrective action can be swiftly taken.

FAILURE RATE PREDICTION

Prediction of the failure rate of CMOS ICs is determined by means of accelerated life testing under carefully monitored conditions that simulate long-term device service. Table XV and Fig. 78 show RCA AC/ACT logic failure rate estimates at various temperatures. The 1.4 FITs (Failure in Time) prediction at 55°C is current as of August 1988. Reliability data will continue to be accumulated over the life of the family.

Table XV - AC/ACT Failure Rates (plastic dual-in-line package). These data cover 1987 and the first half of 1988.

Temperature (°C)	Equivalent Device Hours (A)	Failure Rate FITs (B)
125	7.7×10^6	680
85	2.0×10^8	26
55	3.9×10^9	1.4
Quantity Life Tested (C):	6870	
Quantity Outside Specifications:	4	

(A) Extrapolation based on activation energy of 1.0 eV.
(B) FITs equal failures in 10^9 device hours estimated at a 60% upper confidence level.
(C) Combines bias life data at 175°C and bias plus dynamic life data at 125°C

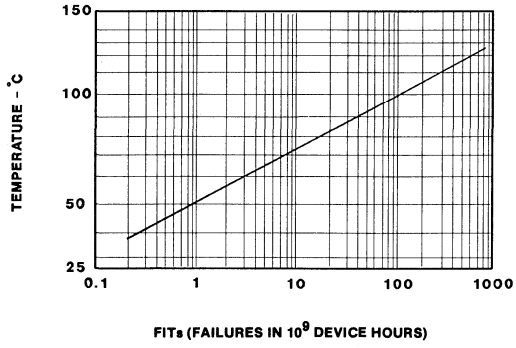


Fig. 78. Failure rate estimate for AC/ACT logic ICs.

RELIABILITY TESTS

Table XVI shows the results of RCA Matrix I reliability test monitors. The highly accelerated test conditions were designed to provide rapid feedback of potential failure mechanisms to the factory. Life tests are conducted at 175°C, which is well above the maximum rated temperature. The HAST (Highly Accelerated Stress Test) is a temperature-humidity-bias environment test that quickly evaluates the moisture-related performance of the plastic package-die system.

Table XVI - Reliability Tests (Matrix I) (plastic dual-in-line package). These data cover 1987 and the first half of 1988.

Test/Conditions	Duration	Units Tested	Devices Outside Specifications
Static Bias Life T_A = 175°C V_{DD} = Rated	48 hours	3720	3 (A)
HAST T_A = 145°C RH = 85% V_{DD} = Rated	20 hours	1800	1 (A)

RH = Relative Humidity
HAST = Highly Accelerated Stress Test
(A) Exceeded parametric limits because of bake-reversible ionic drift.

The results of extended life monitors are shown in Table XVII under Reliability Test Matrix II. The 125°C, bias, and operating life tests are conducted at the maximum rated temperature and voltage for the device. Time is extended to 1000 hours on each sample. Matrix II also contains the industry-standard 85°C, 85% relative humidity, bias life test (THB). This test monitors long-term device performance against data-sheet parameters for operation in a humid environment.

Another plastic-package moisture-penetration test in Matrix II is the "pressure cooker" or autoclave test. In this test the key objective is to try to force moisture into the plastic package. Rejects are those ICs that are out of data-sheet specification and confirmed to have chip metallization corrosion by die inspection. RCA plastic ICs have special lead-frame designs to help retard the entrance of moisture and contaminants.

Table XVII - Extended Life Reliability Tests (Matrix II) (Plastic dual-in-line package). These data cover 1987 and the first half of 1988.

Test/Conditions	Duration	Units Tested	Devices Outside Specifications
Dynamic Life 125°C, 6 V	1000 hours	1250	0
Temperature, Humidity, Bias 85°C, RH = 85%, 6 V	1000 hours	2190	3 (A)
HAST 145°C, RH = 85%, 6 V	20 hours	2440	0
Pressure Cooker 15 psig, 121°C	192 hours	2700	0
Storage Life 150°C	1000 hours	900	0
Temperature Cycle -65°C to +150°C (Air-to-air)	1000 cycles	1200	0
Thermal Shock -65°C to +150°C (Liquid-to-liquid	1000 cycles	2300	0

(A) Exceeded parametric limits; cause undetermined.

Performance degradation caused by a physical mismatch of thermal expansion coefficients between the IC chip and the package materials is detected by the Matrix II temperature cycle and thermal shock tests. RCA plastic-package systems are of such quality that at least 1000 cycles are required to expose a possible thermal expansion problem. The post-test device critique criteria include electrical data-sheet parameters and visible mechanical damage to the package.

In addition to the above tests, physical-package-related tests are periodically monitored. These tests include solderability, lead fatigue, brand adhesion, flammability, and bond pull.

Enhanced Product

FEATURES

Enhanced Advanced CMOS Logic is Burned-In and has a tighter AQL than standard product.

Burn-in Time* - 160 Hours

Bias Voltage - 6 V

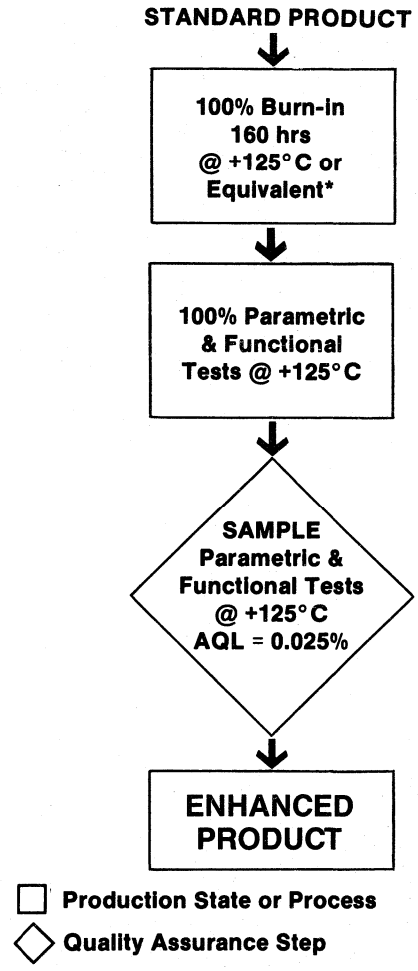
Identification is by an added suffix X to the standard brand.

Examples for the 00 type in the plastic DIP package

CD74AC00EX
or
CD74ACT00EX

*Or equivalent means equivalent time-temperature/voltage resulting in the same activation energy.

PRODUCT FLOW



ENHANCED PRODUCT APPLICATION

The need to achieve the enhanced reliability resulting from burn-in screening must be determined by careful analysis of system design and application.

How many IC's are incorporated into the total system?

How many devices on each board?

Is the proper device being used for the application?

What are the reliability goals?

What failure rates are being experienced without screening?

Cost-effectiveness of using enhanced CMOS can be determined by mutual analysis of the economic trade-offs made possible by the following features of the program:

- Available in plastic package (Dual-In-Line).
- Offered on the industry's broadest line of circuit functions.
- 0.025% AQL cumulative; AQL on standard product is 0.065% cumulative.
- Reduction in PC board reworking through fewer line rejects.
- Lower warranty requirements through the elimination of infant mortality failures.
- Reduced incoming inspection cost by reduction or complete elimination of test procedures.
- Reduction of system failures and related service expenses and customer complaints.

Family Ratings and Specifications

Ratings and Operating Conditions

The absolute maximum ratings, recommended operation conditions, and dc specifications tables of the AC/ACT family are shown on the following pages. Note that the parameter I_{OZ} applies only to three-state and open-drain device types.

Detailed technical information on each individual type is provided in the technical data section.

MAXIMUM RATINGS, *Absolute-Maximum Values:*▲

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For $T_A = -55$ to +100°C (PACKAGE TYPE E) ..... 500 mW
For $T_A = +100$ to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A = -55$ to +70°C (PACKAGE TYPE M) ..... 400 mW
For $T_A = +70$ to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*(For up to 4 outputs per device; add ± 25 mA for each additional output.)

▲Absolute-Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

Specifications

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current▲ I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI† I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.
▲3-State devices only (off-state leakage current for open-drain types).
† SSI/FF limits are 4 μA @ + 25°C, 40 μA @ 0 to +70°C, - 40 to +85°C, 80 μA @ -55 to +125°C.

Specifications

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State or Leakage Current▲ I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI† I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.
▲3-State devices only (off-state leakage current for open-drain types).
† SSI/FF limits are 4 μA @ + 25°C, 40 μA @ 0 to +70°C, - 40 to +85°C, 80 μA @ -55 to +125°C.

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{CC} - Gnd to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{CC} nor less than Gnd. Input currents must not exceed 20 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or Gnd, whichever is appropriate.

Output Short Circuits

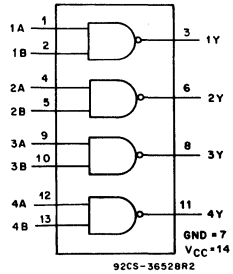
Shorting of outputs to V_{CC} or Gnd may damage CMOS devices by exceeding the maximum device dissipation.

Substrate Connection

When devices in chip form are used in hybrid applications, the substrate is connected to Gnd (as with all p-substrate devices).

Technical Data

CD54/74AC00
CD54/74ACT00



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Quad 2-Input NAND Gate

Type Features:

- *Typical propagation delay (AC00): 3.2ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC00 and CD54/74ACT00 quad 2-input NAND gates use the RCA ADVANCED CMOS technology. The CD74AC00 and CD74ACT00 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC00 and CD54ACT00, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

INPUTS		OUTPUTS
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (PD):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

File Number **1855**

CD54/74AC00
CD54/74ACT00

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC00
CD54/74ACT00

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC00
CD54/74ACT00

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	t_{PLH} t_{PHL}	1.5	—	83	—	91	ns
		3.3*	2.7	9.3	2.6	10.2	
		5†	1.9	6.6	1.8	7.3	
Power Dissipation Capacitance	C_{PD}§	—	45 Typ.		45 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

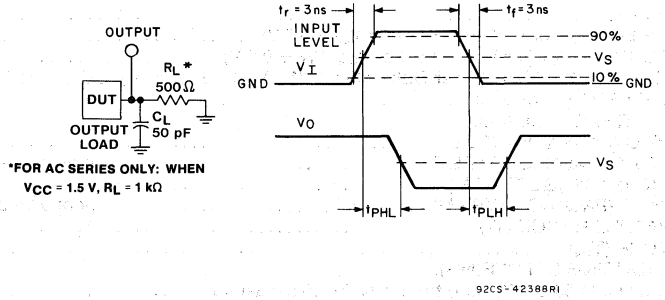
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	t_{PHL}	5†	2.8	9.8	2.7	10.8	ns
	t_{PLH}	5†	3.4	12	3.3	13.2	
Power Dissipation Capacitance	C_{PD}§	—	45 Typ.		45 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per gate.
For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage



	54/74AC	54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times.

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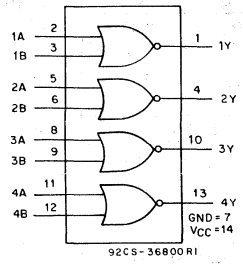
CD54/74AC02
CD54/74ACT02

Advance Information



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Quad 2-Input NOR Gate

Type Features:

- *Typical propagation delay (AC02): 6 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC02 and CD54/74ACT02 quad 2-input NOR gates use the RCA ADVANCED CMOS technology. The CD74AC02 and CD74ACT02 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0° to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC02 and CD54ACT02, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC type features 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

File Number **1978**

CD54/74AC02
CD54/74ACT02

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C: +25 MIN.	+25 MAX.	-40 to +85 MIN.	-40 to +85 MAX.	-55 to +125 MIN.	-55 to +125 MAX.	UNITS
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC02
CD54/74ACT02

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
ALL	0.32

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC02
CD54/74ACT02

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4.1 3	131 14.6 10.4	— 4 2.9	144 16.1 11.5	ns
Power Dissipation Capacitance	C_{PD}§	—	55 Typ.		55 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

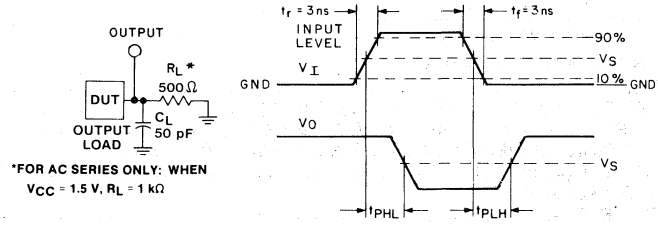
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	t_{PLH} t_{PHL}	5†	3.1	11.1	3.1	12.2	ns
Power Dissipation Capacitance	C_{PD}§	—	55 Typ.		55 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per gate.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.



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	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

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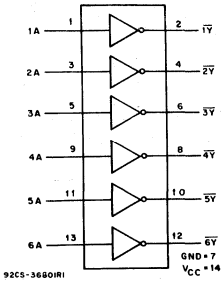
CD54/74AC04, CD54/74AC05
CD54/74ACT04, CD54/74ACT05



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Hex Inverters

CD54/74AC/ACT04 - Active Outputs
CD54/74AC/ACT05 - Open-Drain Outputs

Type Features:

- *Buffered inputs*
- *Typical propagation delay (AC04/05): 3.5 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA-CD54/74AC04, -05 and CD54/74ACT04, -05 hex inverters use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT04 have active outputs; the CD54/74AC/ACT05 have open-drain outputs.

The CD74AC04, -05 and CD74ACT04, -05 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC04, -05 and CD54ACT04, -05, available in chip form (H suffix), are operable over the -55 to +125°C temperature.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

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TRUTH TABLES

CD54/74AC/ACT04

INPUT A	OUTPUT Y
L	H
H	L

CD54/74AC/ACT05

INPUT A	OUTPUT Y
L	Z
H	L

Z = High Impedance

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

File Number **1945**

CD54/74AC04, CD54/74AC05
CD54/74ACT04, CD54/74ACT05

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C: +25 MIN.	+25 MAX.	-40 to +85 MIN.	-40 to +85 MAX.	-55 to +125 MIN.	-55 to +125 MAX.	UNITS
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage (04) V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC04, CD54/74AC05
CD54/74ACT04, CD54/74ACT05

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage (04) V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
nA	0.18

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

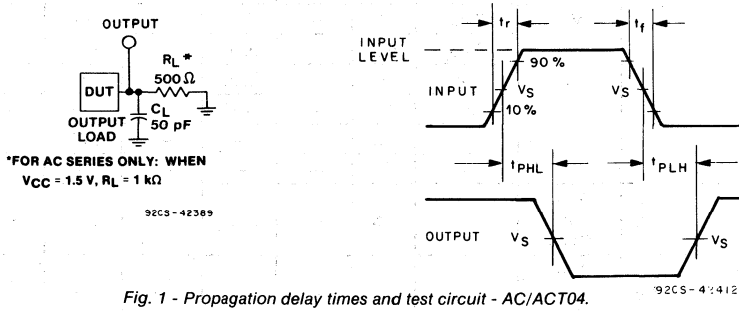


Fig. 1 - Propagation delay times and test circuit - AC/ACT04.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

CD54/74AC04, CD54/74AC05
CD54/74ACT04, CD54/74ACT05

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				-40 to +85		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	(04)	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 2.3 1.7	74 10.4 5.9	— 2.3 1.6	81 9.1 6.5	ns
High Z to Output Low	(05)	t_{PZL}	1.5 3.3 5	— 2.3 1.7	74 10.4 5.9	— 2.3 1.6	81 9.1 6.5	ns
Output Low to High Z	(05)	t_{PLZ}	1.5 3.3 5	— 3 2.2	94 10.4 7.5	— 2.9 2.1	103 11.5 8.2	ns
Power Dissipation Capacitance		C_{PD}§	—	105 Typ.		105 Typ.		pF
Input Capacitance		C_I	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				-40 to +85		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	(04)	t_{PLH} t_{PHL}	5†	2.4	8.5	2.3	9.3	ns
Output Low to High Z		t_{PLZ}	5	2.8	9.8	2.7	10.8	ns
High Z to Output Low	(05)	t_{PZL}	5	2.4	8.5	2.3	9.3	ns
Power Dissipation Capacitance		C_{PD}§	—	105 Typ.		105 Typ.		pF
Input Capacitance		C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per inverter.
For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$, where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

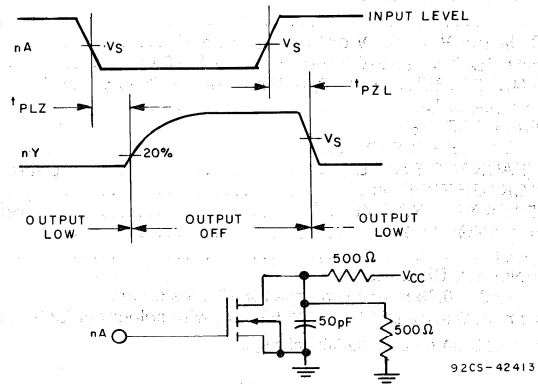
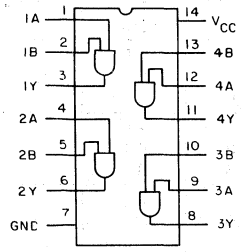


Fig. 2 - Propagation delay times and test circuit - AC/ACT05.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

CD54/74AC08
CD54/74ACT08



92CS-37971

FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Quad 2-Input AND Gate

Type Features:

- *Buffered inputs*
- *Typical propagation delay (AC08): 4.3 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC08 and CD54/74ACT08 quad 2-input AND gates use the RCA ADVANCED CMOS technology. The CD74AC08 and CD74ACT08 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC08 and CD54ACT08, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

TRUTH TABLE

Inputs		Output
nA	nB	nY
L	L	L
H	L	L
L	H	L
H	H	H

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

File Number **1950**

CD54/74AC08
CD54/74ACT08

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
	V_{IH}	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	or	-4	3	2.58	—	2.48	—	2.4	—	
	V_{IL}	-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC08
CD54/74ACT08

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +125		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
	#, *	-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
	#, *	24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
All	0.3

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC08
CD54/74ACT08

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	t_{PLH} t_{PHL}	1.5	—	99	—	109	ns
		3.3*	3.1	11.1	3.1	12.2	
		5†	2.2	7.9	2.2	8.7	
Power Dissipation Capacitance	C_{PD}§	—	50 Typ.		50 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

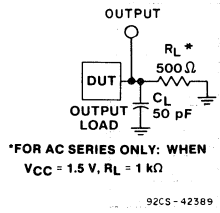
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

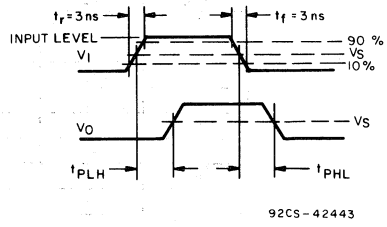
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	t_{PLH} t_{PHL}	5†	3.3	11.7	3.2	12.9	ns
Power Dissipation Capacitance	C_{PD}§	—	50 Typ.		50 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per gate.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_{4i} (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.





	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

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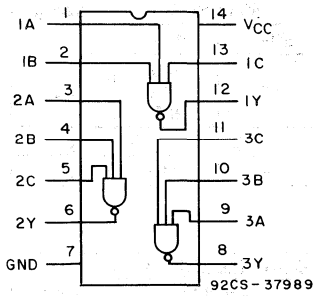
CD54/74AC10
CD54/74ACT10

Advance Information



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Triple 3-Input NAND Gate

Type Features:

- *Typical propagation delay (AC10): 6 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC10 and CD54/74ACT10 triple 3-input NAND gates use the RCA ADVANCED CMOS technology. The CD74AC10 and CD74ACT10 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C). The CD54AC10 and CD54ACT10, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC type features 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

**FAST is a Registered Trademark of Fairchild Semiconductor Corp.*

TRUTH TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

File Number **1977**

CD54/74AC10
CD54/74ACT10

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

9

CD54/74AC10
CD54/74ACT10

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI Icc	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC10
CD54/74ACT10

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
ALL	0.19

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC10
CD54/74ACT10

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	t_{PLH} t_{PHL}	1.5	—	139	—	153	ns
		3.3*	4.4	15.5	4.3	17.1	
		5†	3.1	11.1	3.1	12.2	
Power Dissipation Capacitance	C_{PD}§	—	50 Typ.		50 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

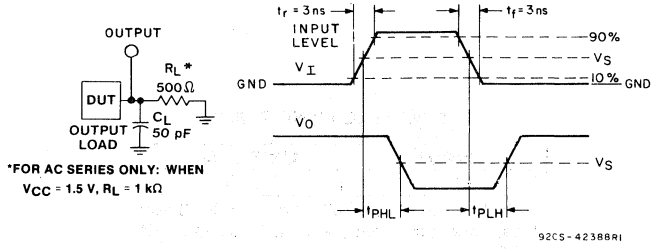
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	t_{PLH} t_{PHL}	5†	3.5	12.3	3.4	13.5	ns
Power Dissipation Capacitance	C_{PD}§	—	50 Typ.		50 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per gate.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

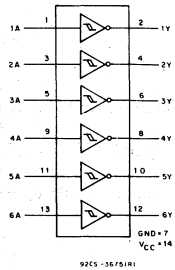


	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

Advance Information

CD54/74AC14
CD54/74ACT14



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Hex Inverting Schmitt Trigger

Type Features:

- *Operates with much slower than standard input rise and fall slew rates*
- *Exceptionally high noise immunity*

The RCA CD54/74AC14 and CD54/74ACT14 each contain six inverting Schmitt Triggers in one package. These devices use the RCA ADVANCED CMOS technology.

The CD74AC14 and CD74ACT14 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC14 and CD54ACT14, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*
- *Greater noise immunity than standard inverters*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

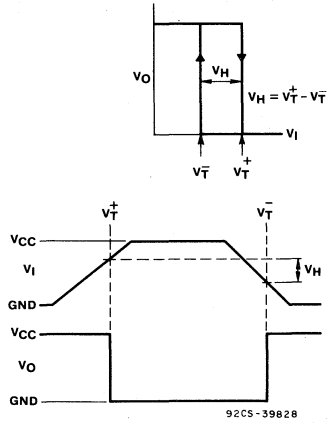


Fig. 1 - Hysteresis definition and characteristic.

TRUTH TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

H = High Level
L = Low Level

9

File Number **1984**

CD54/74AC14
CD54/74ACT14

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv†:			
at 1.5 V to 5.5 V (AC Types)	0	150	ms/V
at 4.5 V to 5.5 V (ACT Types)	0	20	ns/V

*Unless otherwise specified, all voltages are referenced to ground.
†5 Outputs switching
V_{CC} = 5 V
Load = 500Ω, 50 pF
T_A = Full temperature range
For AC14, V_I = 5.5 V sawtooth
For ACT14, V_I = 3 V sawtooth

CD54/74AC14
CD54/74ACT14

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Positive-Going Threshold Voltage V_T^+			5	2.6	3.4	2.6	3.4	2.6	3.4	V
Negative-Going Threshold Voltage V_T^-			5	1.6	2.4	1.6	2.4	1.6	2.4	V
Hysteresis Voltage V_H			5	0.5	—	0.5	—	0.5	—	V
High-Level Output Voltage V_{OH}	V_T^+ or V_T^-	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_T^+ or V_T^-	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND	—	5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current,SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC14
CD54/74ACT14

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Positive-Going Threshold Voltage V_{T^+}			5	1.4	2	1.4	2	1.4	2	V
Negative-Going Threshold Voltage V_{T^-}			5	0.9	1.3	0.9	1.3	0.9	1.3	V
Hysteresis Voltage V_H			5	0.4	—	0.4	—	0.4	—	V
High-Level Output Voltage V_{OH}	V_{T^+} or V_{T^-}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{T^+} or V_{T^-}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND	—	5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current,SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1	—	4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
ALL	0.21

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC14
CD54/74ACT14

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

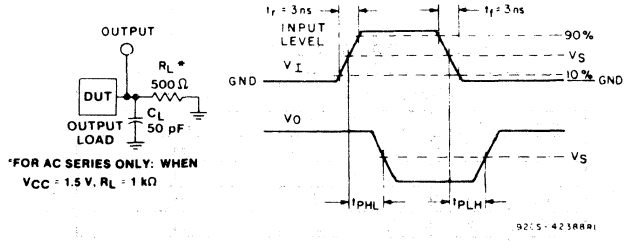
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	t_{PLH} t_{PHL}	5†	2.7	9.5	2.6	10.5	ns
Power Dissipation Capacitance	C_{PD}§	—	45 Typ.		45 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	t_{PLH}	5†	3.7	13.2	3.6	14.5	ns
	t_{PHL}		2.4	8.6	2.4	9.5	
Power Dissipation Capacitance	C_{PD}§	—	45 Typ.		45 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per gate.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.



	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

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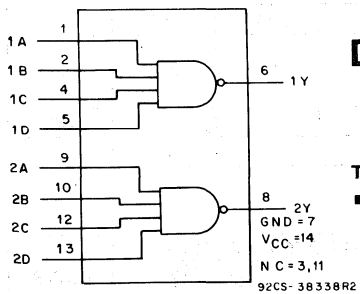
CD54/74AC20
CD54/74ACT20

Advance Information



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Dual 4-Input NAND Gate

Type Features:

- *Typical propagation delay (AC20): 6 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF*

The RCA CD54/74AC20 and CD54/74ACT20 dual 4-input NAND gates use the RCA ADVANCED CMOS technology. The CD74AC20 and CD74ACT20 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +25°C).

The CD54AC20 and CD54ACT20, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS				OUTPUTS
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

X = Don't Care

File Number **1976**

CD54/74AC20
CD54/74ACT20

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
(For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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CD54/74AC20
CD54/74ACT20

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI Icc	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C +25 MIN.	+25 MAX.	-40 to +85 MIN.	-40 to +85 MAX.	-55 to +125 MIN.	-55 to +125 MAX.	UNITS
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

9

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
ALL	0.27

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC20
CD54/74ACT20

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4.4 3.1	139 15.5 11.1	— 4.3 3.1	153 17.1 12.2	ns
Power Dissipation Capacitance	C_{PD}§	—	48 Typ.		48 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

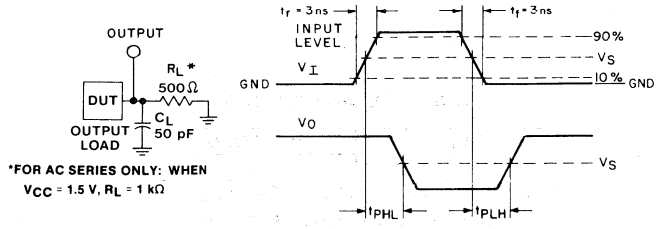
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delay Input to Output	t_{PLH} t_{PHL}	5†	3.5	12.3	3.4	13.5	ns
Power Dissipation Capacitance	C_{PD}§	—	48 Typ.		48 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per gate.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.



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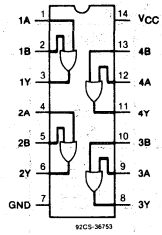
	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

Advance Information

CD54/74AC32
CD54/74ACT32



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Quad 2-Input OR Gate

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 4.5 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF*

The RCA-CD54/74AC32 and CD54/74ACT32 quad 2-input OR gates use the RCA ADVANCED CMOS technology. The CD74AC32 and CD74ACT32 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC32 and CD54ACT32, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

9

File Number **1951**

CD54/74AC32
CD54/74ACT32

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC32
CD54/74ACT32

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin, TTL Inputs High, 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5		2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
ALL	0.42

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC32
CD54/74ACT32

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	t_{PLH} t_{PHL}	1.5	—	108	—	119	ns
		3.3*	3.4	12.1	3.3	13.3	
		5†	2.4	8.6	2.4	9.5	
Power Dissipation Capacitance	C_{PD}§	—	47 Typ.		47 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

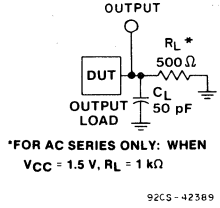
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

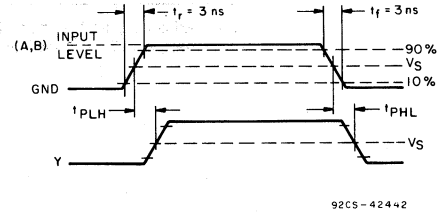
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Output	t_{PLH} t_{PHL}	5†	3.1	11	3	12.1	ns
Power Dissipation Capacitance	C_{PD}§	—	47 Typ.		47 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per gate.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

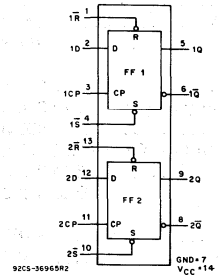




	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

CD54/74AC74
CD54/74ACT74



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Dual D-type Flip-Flop with Set and Reset
Positive-Edge-Triggered

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 4.9 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF*

The RCA CD54/74AC74 and CD54/74ACT74 dual D-type, positive-edge-triggered flip-flops use the RCA ADVANCED CMOS technology. These flip-flops have independent DATA, $\overline{SET}$, $\overline{RESET}$, and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

The CD74AC/ACT74 types are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC74 and CD54ACT74, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:
- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	⎍	H	H	L
H	H	⎍	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H = High level (steady state), L = Low level (steady state), X = Don't care, ⎍ = Transition from Low to High level

NOTES: QO = the level of Q before the indicated input conditions were established.
*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

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File Number **1881**

CD54/74AC74
CD54/74ACT74

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +120°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, FF I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC74
CD54/74ACT74

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	±0.1	—	±1	—	±1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, FF I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5		2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
D	0.53
$\overline{R}$, $\overline{S}$	0.58
CP	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC74
CD54/74ACT74

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t_{SU}	1.5	39	—	44	—	ns
		3.3*	4.3	—	4.9	—	
		5†	3.1	—	3.5	—	
Hold Time	t_H	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
Removal Time $\overline{R}$, $\overline{S}$ to CP	t_{REM}	1.5	30	—	34	—	ns
		3.3	4.1	—	4.7	—	
		5	2.4	—	2.7	—	
Pulse Width $\overline{R}$, $\overline{S}$	t_W	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	
Pulse Width CP	t_W	1.5	49	—	56	—	ns
		3.3	5.5	—	6.3	—	
		5	3.9	—	4.5	—	
CP Frequency	f_{MAX}	1.5	10	—	9	—	MHz
		3.3	90	—	79	—	
		5	125	—	110	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series, t_r t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1.5	—	114	—	125	ns
		3.3*	3.6	12.7	3.5	14	
		5†	2.6	9.1	2.5	10	
$\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$	t_{PLH}	1.5	—	120	—	132	ns
		3.3	3.8	13.4	3.7	14.7	
		5	2.7	9.5	2.6	10.5	
	t_{PHL}	1.5	—	131	—	144	ns
		3.3	4.1	14.6	4	16.1	
		5	3	10.4	2.9	11.5	
Power Dissipation Capacitance	C_{PD}§	—	55 Typ.		55 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC74
CD54/74ACT74

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t_{SU}	5*	3.5	—	4	—	ns
Hold Time	t_H	5	0	—	0	—	ns
Removal Time $\overline{R}$, $\overline{S}$ to CP	t_{REM}	5	2.4	—	2.7	—	ns
Pulse Width $\overline{R}$, $\overline{S}$	t_W	5	4.4	—	5	—	ns
Pulse Width CP	t_W	5	5	—	5.7	—	ns
CP Frequency	f_{MAX}	5	97	—	85	—	MHz

*Min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series, t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q, $\overline{Q}$	t_{PLH} t_{PHL}	5*	2.5	8.6	2.4	9.5	ns
$\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$	t_{PLH}	5	3	10.5	2.9	11.5	ns
	t_{PHL}	5	3.2	11.4	3.1	12.5	
Power Dissipation Capacitance	C_{PD}†	—	55 Typ.		55 Typ.		pF
Input Capacitance	C_I	—	—	10	10	—	pF

*Min. is @ 5.5 V
Max. is @ 4.5 V.

†C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

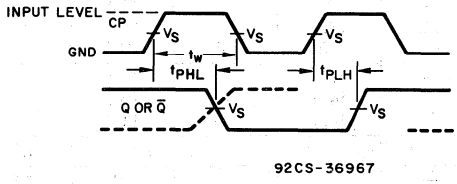


Fig. 1 - Clock prerequisite and propagation delays.

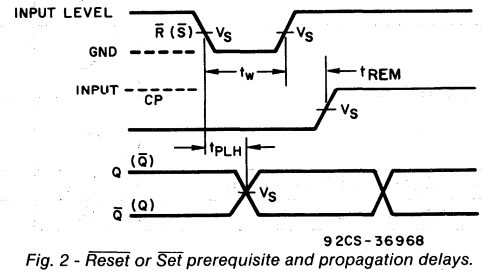
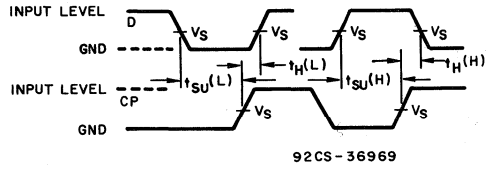


Fig. 2 - $\overline{Reset}$ or $\overline{Set}$ prerequisite and propagation delays.



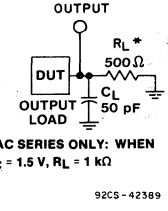
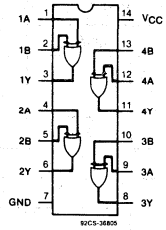


Fig. 3 - Data prerequisite times.

	CD54/74AC	CD54/74ACT
Input Level	V_{cc}	3 V
Input Switching Voltage, Vs	0.5 V_{cc}	1.5 V
Output Switching Voltage, Vs	0.5 V_{cc}	0.5 V_{cc}

Advance Information

CD54/74AC86
CD54/74ACT86



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Quad 2-Input Exclusive-OR Gate

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  3.2 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA CD54/74AC86 and CD54/74ACT86 quad 2-input Exclusive-OR gates use the RCA ADVANCED CMOS technology. The CD74AC86 and CD74ACT86 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC86 and CD54ACT86, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
H	H	L
H	L	H
L	H	H

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265° C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300° C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

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File Number **1952**

CD54/74AC86
CD54/74ACT86

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC86
CD54/74ACT86

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, SSI I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5		2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
ALL	0.48

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC86
CD54/74ACT86

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Outputs	t_{PLH}	1.5	—	123	—	135	ns
	t_{PHL}	3.3*	3.9	13.7	3.8	15.1	
		5†	2.8	9.8	2.7	10.8	
Power Dissipation Capacitance	C_{PD}§	—	57 Typ.		57 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

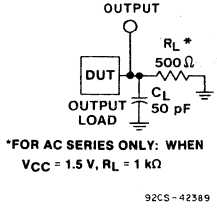
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

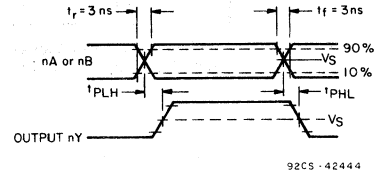
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Input to Outputs	t_{PLH} t_{PHL}	5†	3.8	13.3	3.7	14.6	ns
Power Dissipation Capacitance	C_{PD}§	—	57 Typ.		57 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per gate.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.



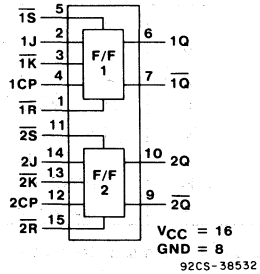


	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

Advanced Information

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112



CD54/74AC/ACT109 FUNCTIONAL DIAGRAM

Dual "J-K" Flip-Flop with Set and Reset

CD54/74AC/ACT109 - Positive-Edge-Triggered (J, $\overline{K}$)
CD54/74AC/ACT112 - Negative-Edge-Triggered (J, K)

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  4.8 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA CD54/74AC109 and CD54/74AC112 and the CD54/74ACT109 and CD54/74ACT112 dual "J-K" flip-flops with set and reset use the RCA ADVANCED CMOS technology. These flip-flops have independent J, K (or $\overline{K}$), Set, Reset, and Clock inputs and Q and $\overline{Q}$ outputs. The CD54/74AC/ACT112 changes state on the negative-going transition of the clock pulse. The CD54/74AC/ACT109 changes state on the positive-going transition of the clock. Set and Reset are accomplished asynchronously by low-level inputs.

The CD74AC/ACT109 and CD74AC/ACT112 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT109 and CD54AC/ACT112, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

CD54/74AC/ACT109 TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↓	H	L	TOGGLE	
H	H	↓	L	H	NO CHANGE	
H	H	↓	H	H	H	L
H	H	L	X	X	NO CHANGE	

*Unpredictable and unstable condition if both $\overline{S}$ and $\overline{R}$ go high simultaneously.

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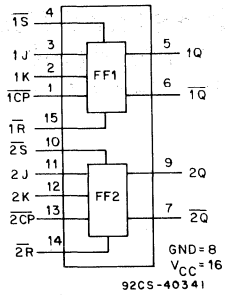
File Number **1967**

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112



CD54/74AC/ACT112 FUNCTIONAL DIAGRAM

CD54/74AC/ACT112 TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{S}$	$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	NO CHANGE	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	NO CHANGE	

*Output states unpredictable if $\overline{S}$ and $\overline{R}$ go High simultaneously after both being Low at the same time.
H = High steady state
L = Low steady state
X = Irrelevant

↓ = High-to-Low transition

↑ = Low-to-High transition

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

STATIC ELECTRICAL CHARACTERISTICS: AC Series

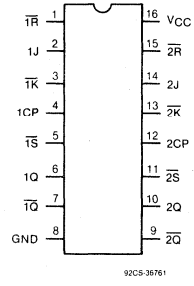
CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, FF I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

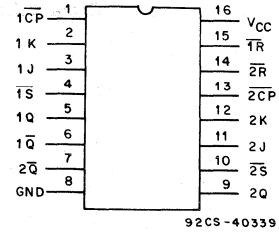
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

9

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT109



CD54/74AC/ACT112

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.10	—	0.10	—	0.10	V
		24	4.5	—	0.36	—	0.44	—	0.50	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, FF I_{CC}	V_{CC} or GND	0	5.5	—	4	—	40	—	80	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*	
	109	112
J, CP, $\overline{CP}$	1	1
K	—	0.53
$\overline{K}$	0.53	—
$\overline{S}$, $\overline{R}$	0.58	0.58

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum CP, ($\overline{CP}$) Frequency		1.5	9	—	8	—	
109	f_{max}	3.3*	81	—	71	—	MHz
		5†	114	—	100	—	
		1.5	9	—	8	—	
112	f_{max}	3.3	81	—	71	—	MHz
		5	114	—	100	—	
CP, ($\overline{CP}$) Pulse Width		1.5	55	—	63	—	
	t_W	3.3	6	—	7	—	ns
		5	4.4	—	5	—	
$\overline{R}$, $\overline{S}$ Pulse Width		1.5	49	—	56	—	
	t_W	3.3	5.5	—	6.3	—	ns
		5	3.9	—	4.5	—	
Setup Time		1.5	61	—	69	—	
J, $\overline{K}$ to CP	t_{SU}	3.3	6.8	—	7.7	—	ns
109		5	4.8	—	5.5	—	
		1.5	44	—	50	—	
J, K to $\overline{CP}$	t_{SU}	3.3	4.9	—	5.6	—	ns
112		5	3.5	—	4	—	
Hold Time		1.5	0	—	0	—	
J, $\overline{K}$ to CP	t_H	3.3	0	—	0	—	ns
109		5	0	—	0	—	
		1.5	0	—	0	—	
J, K to $\overline{CP}$	t_H	3.3	0	—	0	—	ns
112		5	0	—	0	—	
Removal Time		1.5	27	—	31	—	
$\overline{R}$, $\overline{S}$ to CP, ($\overline{CP}$)	t_{REM}	3.1	3.1	—	3.5	—	ns
		5	2.2	—	2.5	—	

*3.3 V: min. is @ 3 V
†5 V: min is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:		1.5	—	117	—	129	
CP, ($\overline{CP}$) to Q, $\overline{Q}$	t_{PLH}	3.3*	3.7	13.1	3.6	14.4	ns
	t_{PHL}	5†	2.7	9.4	2.6	10.3	
	t_{PLH}	1.5	—	139	—	153	
$\overline{S}$, R to Q, $\overline{Q}$	t_{PLH}	3.3	4.4	15.5	4.3	17.1	ns
	t_{PHL}	5	3.2	11.1	3.1	12.2	
Power Dissipation Capacitance	C_{PD}§	—	56 Typ.		56 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

† 5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum CP, ($\overline{CP}$) Frequency 109	f_{max}	5*	114	—	100	—	MHz
112			114	—	100	—	
CP, ($\overline{CP}$) Pulse Width	t_W	5	4.4	—	5	—	ns
$\overline{R}$, $\overline{S}$ Pulse Width	t_W	5	4.8	—	5.5	—	ns
Setup Time J, $\overline{K}$ to CP (109)	t_{SU}	5	4.8	—	5.5	—	ns
J, K to $\overline{CP}$ (112)			3.5	—	4	—	
Hold Time J, $\overline{K}$ to CP (109)	t_H	5	0	—	0	—	ns
J, K to $\overline{CP}$ (112)			1	—	1	—	
Removal Time $\overline{R}$, $\overline{S}$ to CP, ($\overline{CP}$)	t_{REM}	5	2.2	—	2.5	—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

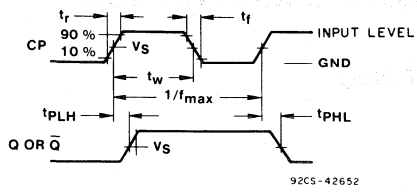
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays CP, ($\overline{CP}$) to Q, $\overline{Q}$	t_{PLH} t_{PHL}	5*	2.7	9.4	2.6	10.3	ns
$\overline{S}$, $\overline{R}$, to Q, $\overline{Q}$	t_{PLH} t_{PHL}	5	3.2	11.1	3.1	12.2	ns
Power Dissipation Capacitance	C_{PD}§	—	56 Typ.		56 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

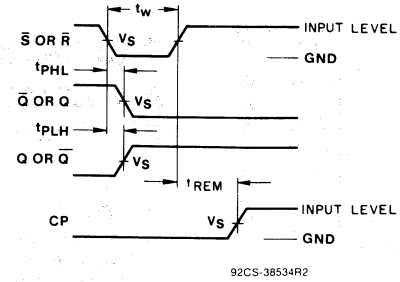
§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC109, CD54/74AC112
CD54/74ACT109, CD54/74ACT112

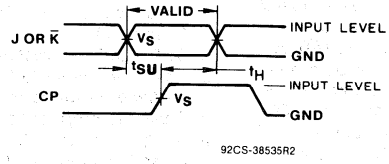
CD54/74AC/ACT109 Waveforms



Clock to output delays and clock pulse width.

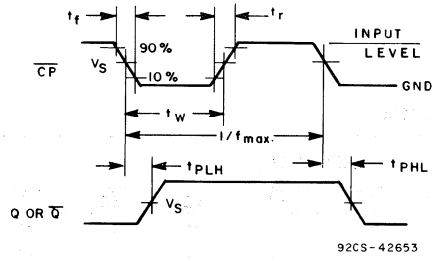


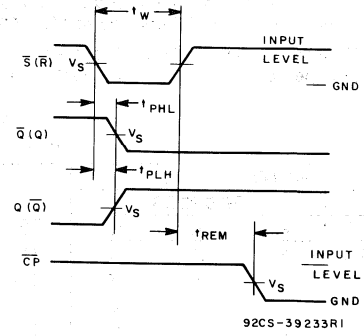
$\overline{\text{Reset}}$ or $\overline{\text{Set}}$ prerequisite and propagation delays.

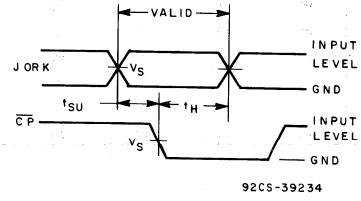


Data setup and hold times.

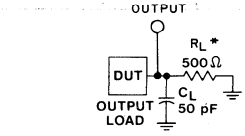
CD54/74/AC/ACT112 Waveforms







Propagation delay times, and setup and hold times.



Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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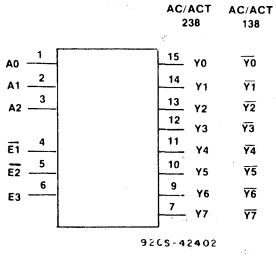
CD54/74AC138, CD54/74AC238
CD54/74ACT138, CD54/74ACT238

Advance Information



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

3-to-8-Line Decoders/Demultiplexers

AC/ACT138 - Inverting
AC/ACT238 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay (AC/ACT138): 5 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA-CD54/74AC138 and CD54/74AC238 and the CD54/74ACT138 and CD54/74ACT238 3-to-8-line decoders/demultiplexers use the RCA ADVANCED CMOS technology. Both circuits have three binary select inputs (A0, A1, and A2). If the device is enabled, these inputs determine which one of the eight normally HIGH outputs of the AC/ACT138 will go LOW or which one of the normally LOW outputs of the AC/ACT238 will go HIGH. Two active LOW and one active HIGH enables ($\overline{E1}$, $\overline{E2}$, and E3) are provided to simplify the cascading of these devices.

The CD74AC/ACT138 and CD74AC/ACT238 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT138 and CD54AC/ACT238, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE
CD54/74AC138, CD54/74ACT138

INPUTS					OUTPUTS							
ENABLE		ADDRESS										
E_3	$*\overline{E}_0$	A_2	A_1	A_0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = High level, L = Low level, X = Don't care
$*\overline{E}_0 = \overline{E}_1 + \overline{E}_2$

File Number **1909**

CD54/74AC138, CD54/74AC238
CD54/74ACT138, CD54/74ACT238

TRUTH TABLE
CD54/74AC238, CD54/74ACT238

INPUTS					OUTPUTS							
ENABLE		ADDRESS										
E_3	$*\overline{E_0}$	A2	A_1	A_0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	H	H	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

H = High level, L = Low level, X = Don't care
$*\overline{E_0} = \overline{E_1} + \overline{E_2}$

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

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RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC138, CD54/74AC238
CD54/74ACT138, CD54/74ACT238

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC138, CD54/74AC238
CD54/74ACT138, CD54/74ACT238

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
	#, *	-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
	#, *	24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
A0 - A2	0.83
$\overline{E1}$, $\overline{E2}$	1
E3	0.42

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC138, CD54/74AC238
CD54/74ACT138, CD54/74ACT238

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
An to Output (138)	t_{PLH}	1.5	—	125	—	138	ns
	t_{PHL}	3.3*	4	14	3.9	15.4	
		5†	2.8	10	2.8	11	
$\overline{E1}$, $\overline{E2}$ to Output (138)	t_{PLH}	1.5	—	114	—	125	ns
	t_{PHL}	3.3	3.6	12.7	3.5	14	
		5	2.6	9.1	2.5	10	
E3 to Output (138)	t_{PLH}	1.5	—	125	—	138	ns
	t_{PHL}	3.3	4	14	3.9	15.4	
		5	2.8	10	2.8	11	
An to Output (238)	t_{PLH}	1.5	—	170	—	187	ns
	t_{PHL}	3.3	5.4	19.1	5.3	21	
		5	3.9	13.6	3.8	15	
$\overline{E1}$, $\overline{E2}$ to Output (238)	t_{PLH}	1.5	—	135	—	149	ns
	t_{PHL}	3.3	4.3	15.2	4.2	16.7	
		5	3.1	10.7	3	11.9	
E3 to Output (238)	t_{PLH}	1.5	—	189	—	208	ns
	t_{PHL}	3.3	6	21.1	5.8	23.2	
		5	4.3	15.1	4.2	16.6	
Power Dissipation Capacitance	C_{PD}‡	—	110 Typ.		110 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
An to Output (138)	t_{PLH}	5†	3.1	10.9	3	12	ns
	t_{PHL}						
$\overline{E1}$, $\overline{E2}$ to Output (138)	t_{PLH}	5	2.7	9.5	2.6	10.5	ns
	t_{PHL}						
E3 to Output (138)	t_{PLH}	5	2.8	10	2.8	11	ns
	t_{PHL}						
An to Output (238)	t_{PLH}	5	4	14.2	3.9	15.6	ns
	t_{PHL}						
$\overline{E1}$, $\overline{E2}$ to Output (238)	t_{PLH}	5	3.7	12.9	3.6	14.2	ns
	t_{PHL}						
E3 to Output (238)	t_{PLH}	5	3.5	12.4	3.4	13.6	ns
	t_{PHL}						
Power Dissipation Capacitance	C_{PD}‡	—	110 Typ.		110 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

‡C_{PD} is used to determine the dynamic power consumption, per package.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC138, CD54/74AC238
CD54/74ACT138, CD54/74ACT238

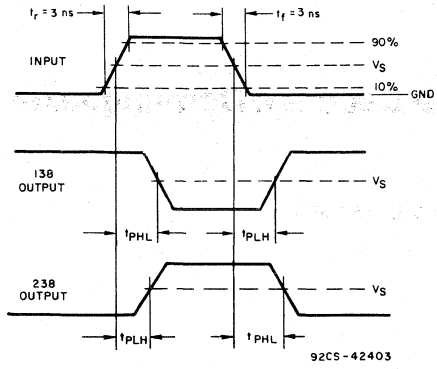

Fig. 1 - Propagation delay times.

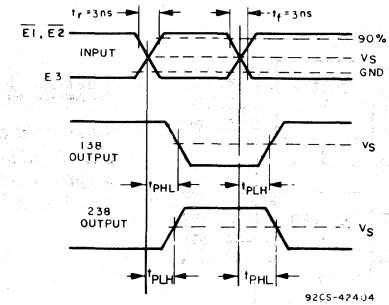

Fig. 2 - Propagation delay times.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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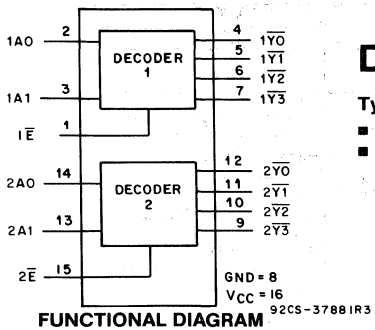
CD54/74AC139
CD54/74ACT139



FUNCTIONAL DIAGRAM

Dual 2-to-4-Line Decoder/Demultiplexer

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  5.4 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA CD54/74AC139 and CD54/74ACT139 dual 2-to-4-line decoders/demultiplexers use the RCA ADVANCED CMOS technology. These devices contain two independent binary to one-of-four decoders, each with a single active-LOW enable input ($\overline{1E}$ or $\overline{2E}$). Data on the select inputs (1A0 and 1A1 or 2A0 and 2A1) cause one of the four normally HIGH outputs to go LOW.

If the enable input is HIGH, all four outputs remain HIGH. For demultiplexer operation, the enable input is the data input. The enable input also functions as a chip select when these devices are cascaded.

The CD74AC139 and CD74ACT139 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC139 and CD54ACT139, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS			
Enable	Select					
$\overline{E}$	A1	A0	$\overline{Y3}$	$\overline{Y2}$	$\overline{Y1}$	$\overline{Y0}$
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H
H	X	X	H	H	H	H

X = Don't care

File Number **1953**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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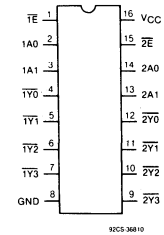

TERMINAL ASSIGNMENT

CD54/74AC139
CD54/74ACT139

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC139
CD54/74ACT139

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin, TTL Inputs High, 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5		2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
A0, A1	1
$\overline{E}$	0.67

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC139
CD54/74ACT139

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A0, A1 to Outputs	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 3.9 2.8	119 13.4 9.5	— 3.7 2.6	131 14.7 10.5	ns
$\overline{E}$ to Outputs	t_{PLH} t_{PHL}	1.5 3.1 5	— 3.9 2.8	119 13.4 9.5	— 3.7 2.6	131 14.7 10.5	ns
Power Dissipation Capacitance	C_{PD}§	—	83 Typ.		83 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

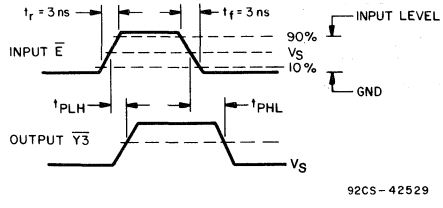
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

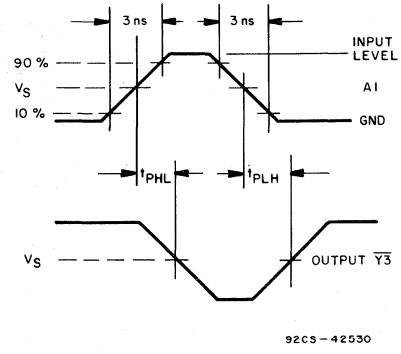
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A0, A1 to Outputs	t_{PLH} t_{PHL}	5†	3.1	10.5	2.9	11.5	ns
$\overline{E}$ to Outputs	t_{PLH} t_{PHL}	5	3.2	10.9	3	12	ns
Power Dissipation Capacitance	C_{PD}§	—	83 Typ.		83 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

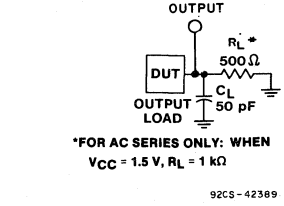
*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per decoder/demultiplexer.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.





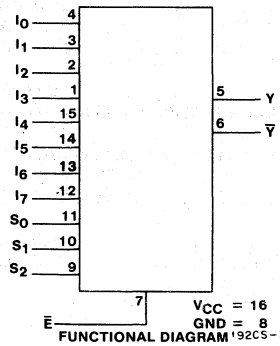


	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

Advance Information

CD54/74AC151
CD54/74ACT151



FUNCTIONAL DIAGRAM '92CS-38431

8-Input Multiplexer

Type Features:
- *Buffered inputs*
- *Typical propagation delay: 6 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC151 and CD54/74ACT151 8-input digital multiplexers use the RCA ADVANCED CMOS technology. They have three binary control inputs (S0, S1, and S2) and an active-LOW Enable ($\overline{E}$) input. The three binary inputs select 1 of 8 channels. The output is both inverting ($\overline{Y}$) and non inverting (Y).

The CD74AC151 and CD74ACT151 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC151 and CD54ACT151, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:
- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

**FAST is a Registered Trademark of Fairchild Semiconductor Corp.*

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level. L = LOW voltage level. X = Don't care.

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File Number **1980**

CD54/74AC151
CD54/74ACT151

MAXIMUM RATINGS, *Absolute-Maximum Values:*

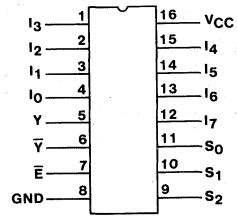
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.



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TERMINAL ASSIGNMENT

CD54/74AC151
CD54/74ACT151

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC151
CD54/74ACT151

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{cc}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
I (All)	1
$\overline{E}$	1
S	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Data to Y	t_{PLH} t_{PHL}	1.5	—	152	—	169	ns
		3.3*	4.9	17.1	4.7	18.9	
		5†	3.5	12.3	3.4	13.5	
Any Data to $\overline{Y}$	t_{PLH} t_{PHL}	1.5	—	169	—	186	ns
		3.3	5.4	19	5.2	20.9	
		5	3.8	13.5	3.7	14.9	
Any Select to Y	t_{PLH} t_{PHL}	1.5	—	207	—	228	ns
		3.3	6.6	23.2	6.4	25.5	
		5	4.7	16.5	4.6	18.2	
Any Select to $\overline{Y}$	t_{PLH} t_{PHL}	1.5	—	223	—	245	ns
		3.3	7.1	24.9	6.9	27.4	
		5	5.1	17.8	4.9	19.6	
Any $\overline{Enable}$ to Y	t_{PLH} t_{PHL}	1.5	—	139	—	153	ns
		3.3	4.4	15.5	4.3	17.1	
		5	3.1	11.1	3.1	12.2	
Any $\overline{Enable}$ to $\overline{Y}$	t_{PLH} t_{PHL}	1.5	—	153	—	169	ns
		3.3	4.9	17.2	4.7	18.9	
		5	3.5	12.3	3.4	13.5	
Power Dissipation Capacitance	C_{PD}§	—	120 Typ.		120 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Data to Y	t_{PLH} t_{PHL}	5*	4	14.1	3.9	15.5	ns
Any Data to $\overline{Y}$	t_{PLH} t_{PHL}	5	4.4	15.4	4.2	16.9	ns
Any Select to Y	t_{PLH} t_{PHL}	5	5.2	18.4	5.1	20.2	ns
Any Select to $\overline{Y}$	t_{PLH} t_{PHL}	5	5.6	19.6	5.4	21.6	ns
Any $\overline{Enable}$ to Y	t_{PLH} t_{PHL}	5	3.1	11	3	12.1	ns
Any $\overline{Enable}$ to $\overline{Y}$	t_{PLH} t_{PHL}	5	3.5	12.3	3.4	13.5	ns
Power Dissipation Capacitance	C_{PD}§	—	120 Typ.		120 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC151
CD54/74ACT151

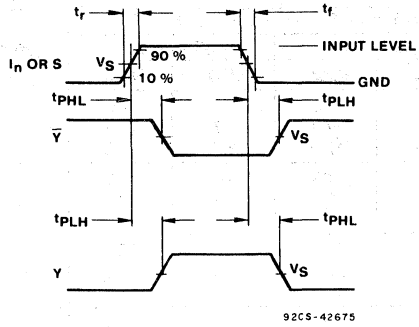


Fig. 1 - Inputs or select to output propagation delays.

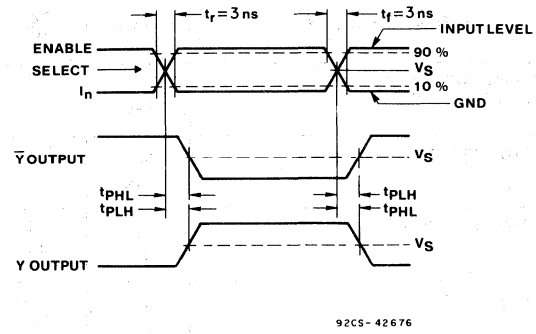


Fig. 2 - Enable to output propagation delays.

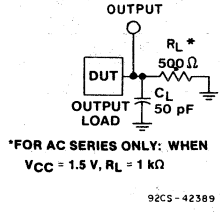
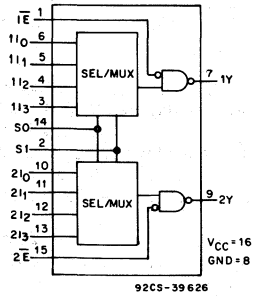


Fig. 3 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Advance Information

CD54/74AC153
CD54/74ACT153



FUNCTIONAL DIAGRAM

Dual 4-Input Multiplexer

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  6.3 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA CD54/74AC153 and CD54/74ACT153 dual 4-input multiplexers use the RCA ADVANCED CMOS technology. One of the four sources for each section is selected by the common Select inputs, S0 and S1. When the Enable inputs ($\overline{1E}$, $\overline{2E}$) are HIGH, the outputs are in the low state.

The CD74AC153 and CD74ACT153 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC153 and CD54ACT153, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

**FAST is a Registered Trademark of Fairchild Semiconductor Corp.*

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				ENABLE INPUTS	OUTPUT
S1	S0	nI_0	nI_1	nI_2	nI_3	$\overline{nE}$	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs S1 and S0 are common to both sections.
H = High level
L = Low level
X = Don't care
Z = High impedance

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File Number **1966**

CD54/74AC153
CD54/74ACT153

MAXIMUM RATINGS, *Absolute-Maximum Values:*

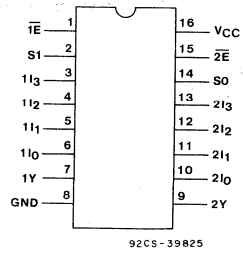
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC153
CD54/74ACT153

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
S0, S1, nI_0, nI_1	1
$\overline{nE}$	0.47

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: S0, S1, to Y	t_{PLH} t_{PHL}	1.5	—	227	—	250	ns
		3.3*	7.2	25.5	7	28	
		5†	5.2	18.2	5	20	
nI to Y	t_{PLH} t_{PHL}	1.5	—	151	—	166	ns
		3.3	4.8	16.9	4.7	18.6	
		5	3.4	12.1	3.3	13.3	
$\overline{nE}$ to Y	t_{PLH} t_{PHL}	1.5	—	134	—	148	ns
		3.3	4.3	15	4.1	16.5	
		5	3.1	10.7	3	11.8	
Power Dissipation Capacitance	C_{PD}§	—	93 Typ.		93 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: S0, S1, to Y	t_{PLH} t_{PHL}	5†	5.7	20	5.5	22	ns
nI to Y	t_{PLH} t_{PHL}	5	4.6	16.4	4.5	18	ns
$\overline{nE}$ to Y	t_{PLH} t_{PHL}	5	3.2	11.5	3.2	12.6	ns
Power Dissipation Capacitance	C_{PD}§	—	93 Typ.		93 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

9

CD54/74AC153
CD54/74ACT153

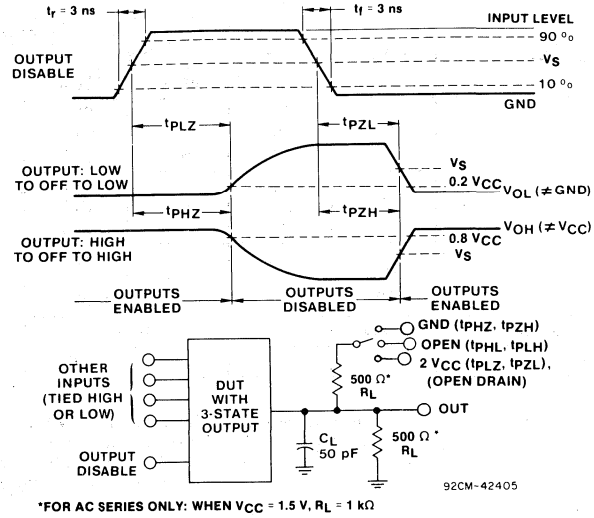


Fig. 1 - Three-state propagation delay waveforms and test circuit.

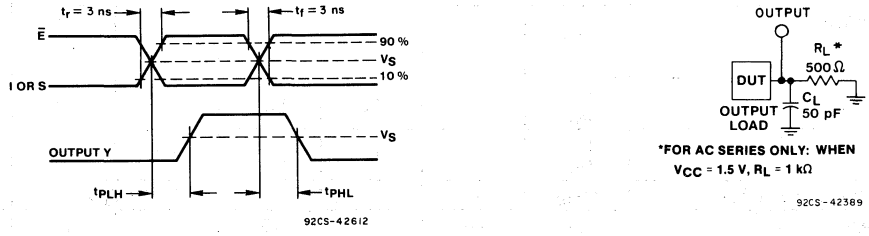
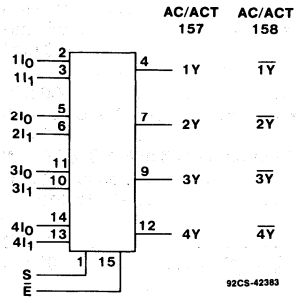


Fig. 2 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

CD54/74AC157, CD54/74AC158
CD54/74ACT157, CD54/74ACT158



FUNCTIONAL DIAGRAM

Quad 2-Input Multiplexers

AC/ACT157 - Non-Inverting
AC/ACT158 - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay (AC/ACT158): 3.8 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC157, -158 and CD54/74ACT157, -158 quad 2-input multiplexers use the RCA ADVANCED CMOS technology. Both circuits can select four bits of data from two sources under the control of a common select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs of the 158 are forced HIGH and in the 157, all of the outputs are forced LOW, regardless of all other input conditions.

The CD74AC/ACT157 and CD74AC/ACT158 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC157, -158 and CD54ACT157, -158, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

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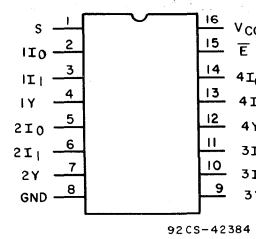
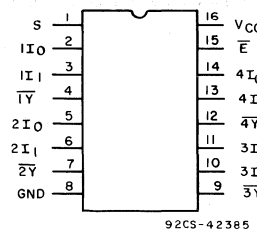
TRUTH TABLE

Enable	Select Input	Data Inputs		Output	
				157	158
$\overline{E}$	S	I_0	I_1	Y	$\overline{Y}$
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High level, L = Low level, X = Don't care



CD54/74AC/ACT157



CD54/74AC/ACT158

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File Number **1910**

CD54/74AC157, CD54/74AC158
CD54/74ACT157, CD54/74ACT158

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC157, CD54/74AC158
CD54/74ACT157, CD54/74ACT158

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC157, CD54/74AC158
CD54/74ACT157, CD54/74ACT158

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	157	158
I (All)	0.37	0.37
$\overline{E}$	0.83	0.83
S	1.33	1.33

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC157, CD54/74AC158
CD54/74ACT157, CD54/74ACT158

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				-40 to +85		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	(157)	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 3.2 2.2	97 10.8 7.7	— 3 2.1	106 11.9 8.5	ns
$\overline{\text{Enable}}$ to Output	(157)	t_{PLH} t_{PHL}	1.5 3.3 5	— 5.1 3.6	154 17.2 12.3	— 4.7 3.4	169 18.9 13.5	ns
Select to Output	(157)	t_{PLH} t_{PHL}	1.5 3.3 5	— 5.4 3.8	164 18.5 13.2	— 5.1 3.6	180 20.3 14.5	ns
Data to Output	(158)	t_{PLH} t_{PHL}	1.5 3.3 5	— 3 2.2	91 12.8 7.3	— 2.8 2	100 11.2 8	ns
$\overline{\text{Enable}}$ to Output	(158)	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.5 3.2	135 15.2 10.8	— 4.2 3	149 16.7 11.9	ns
Select to Output	(158)	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.9 3.5	147 16.5 11.7	— 4.5 3.2	161 18.1 12.9	ns
Power Dissipation Capacitance	(157) (158)	C_{PD}§	—	156 Typ. 149 Typ.		156 Typ. 149 Typ.		pF
Input Capacitance		C_I	—	—	10	—	10	pF

SWITCHING CHARACTERISTIS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				-40 to +85		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	(157)	t_{PLH} t_{PHL}	5†	2.5	8.6	2.4	9.5	ns
$\overline{\text{Enable}}$ to Output	(157)	t_{PLH} t_{PHL}	5	3.6	12.3	3.4	13.5	ns
Select to Output	(157)	t_{PLH} t_{PHL}	5	3.8	13.2	3.6	14.5	ns
Data to Output	(158)	t_{PLH} t_{PHL}	5	2.4	8.4	2.3	9.2	ns
$\overline{\text{Enable}}$ to Output	(158)	t_{PLH} t_{PHL}	5	3.3	11.3	3.1	12.4	ns
Select to Output	(158)	t_{PLH} t_{PHL}	5	3.6	12.3	3.4	13.5	ns
Power Dissipation Capacitance	(157) (158)	C_{PD}§	—	156 Typ. 149 Typ.		156 Typ. 149 Typ.		pF
Input Capacitance		C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per function.
For AC Series, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o)$
For ACT Series, $P_D = C_{PD}V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$
where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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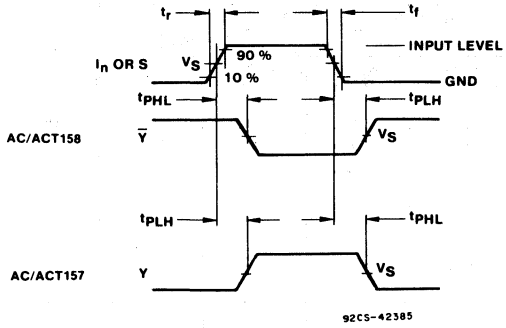
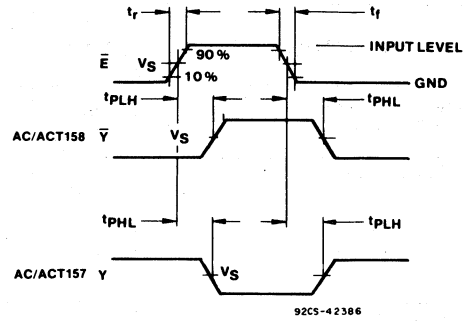
CD54/74AC157, CD54/74AC158
CD54/74ACT157, CD54/74ACT158





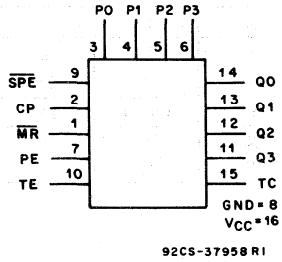
	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 3 - Inputs or select to output propagation delays.

Fig. 4 - $\overline{Enable}$ to output propagation delays.

Advance Information

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163



FUNCTIONAL DIAGRAM

Synchronous Presettable Binary Counters

CD54/74AC/ACT161 - Asynchronous Reset
CD54/74AC/ACT163 - Synchronous Reset

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 7.8 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC161 and CD54/74AC163 and the CD54/74ACT161 and CD54/74ACT163 synchronous presettable binary counters use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT161 are asynchronously reset; the CD54/74AC/ACT163 devices are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A LOW level on the Synchronous Parallel Enable input, $\overline{SPE}$, disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for $\overline{SPE}$ are met).

The counters are reset with a LOW level on the Master Reset input, $\overline{MR}$. In the CD54/74AC/ACT163 counter (synchronous reset), the requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. Reset action occurs regardless of the level of the $\overline{SPE}$, PE, and TE inputs (and the clock input, CP, in the CD54/74AC/ACT161).

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be HIGH to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count, the terminal count (TC) output goes HIGH for one clock period. This TC pulse is used to enable the next cascaded stage.

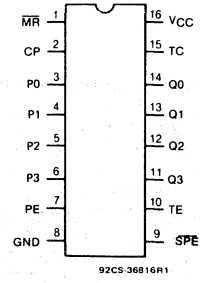
The CD74AC/ACT161 and CD74AC/ACT163 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT161 and CD54AC/ACT163, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.



TERMINAL ASSIGNMENT

9

File Number **1959**

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

MODE SELECT — FUNCTION TABLE (AC/ACT161)

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	⎍	X	X	l	l	L	L
	H	⎍	X	X	l	h	H	(a)
Count	H	⎍	h	h	h	x	count	(a)
Inhibit	H	X	l	X	h	X	q_n	(a)
	H	X	X	l	h	X	q_n	L

MODE SELECT — FUNCTION TABLE (AC/ACT163)

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	l	⎍	X	X	X	X	L	L
Parallel Load	h	⎍	X	X	l	l	L	L
	h	⎍	X	X	l	h	H	(a)
Count	h	⎍	h	h	h	X	count	(a)
Inhibit	h	X	l	X	h	X	q_n	(a)
	h	X	X	l	h	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
q = Lowercase letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
⎍ = LOW-to-HIGH clock transition.

NOTE:
(a) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HHHH).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at+125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Pn	0.13
CP	1
$\overline{MR}$, TE	0.83
$\overline{SPE}$	0.67
PE	0.5

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. CP Frequency	f_{max}	1.5	8	—	7	—	MHz
		3.3*	73	—	64	—	
		5†	103	—	90	—	
CP Pulse Width $\overline{SPE}$ HIGH (Count)	t_W	1.5	61	—	69	—	ns
		3.3	6.8	—	7.7	—	
		5	4.8	—	5.5	—	
$\overline{SPE}$ LOW (Load)	t_W	1.5	61	—	69	—	ns
		3.3	6.8	—	7.7	—	
		5	4.8	—	5.5	—	
$\overline{MR}$ Pulse Width (161)	t_W	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
Setup Time Pn to CP	t_{SU}	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
PE or TE to CP	t_{SU}	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
$\overline{SPE}$ or $\overline{MR}$ to CP (163)	t_{SU}	1.5	66	—	75	—	ns
		3.3	7.4	—	8.4	—	
		5	5.3	—	6	—	
Hold Time Pn to CP	t_H	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
PE or TE to CP	t_H	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
$\overline{SPE}$ or $\overline{MR}$ to CP (163)	t_H	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
Recovery Time $\overline{MR}$ to CP (161)	t_{REC}	1.5	66	—	75	—	ns
		3.3	7.4	—	8.4	—	
		5	5.3	—	6	—	

*3.3 V: min. is @ 3 V
†5 V: min is @ 4.5 V

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CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
CP to Qn	t_{PLH}	1.5	—	188	—	207	
	t_{PHL}	3.3*	5.9	21	5.8	23.1	ns
($\overline{SPE}$ HIGH)		5†	4.2	15	4.1	16.5	
CP to Qn	t_{PLH}	1.5	—	188	—	207	
	t_{PHL}	3.3	5.9	21	5.8	23.1	ns
($\overline{SPE}$ LOW)		5	4.2	15	4.1	16.5	
CP to TC	t_{PLH}	1.5	—	190	—	209	
	t_{PHL}	3.3	6	21	5.9	23.4	ns
		5	4.3	15.2	4.2	16.7	
TE to TC	t_{PLH}	1.5	—	117	—	129	
	t_{PHL}	3.3	3.7	13.1	3.6	14.4	ns
		5	2.7	9.4	2.6	10.3	
$\overline{MR}$ to Qn	t_{PLH}	1.5	—	188	—	207	
(161)	t_{PHL}	3.3	5.9	21	5.8	23.1	ns
		5	4.2	15	4.1	16.5	
$\overline{MR}$ to TC	t_{PLH}	1.5	—	188	—	207	
(161)	t_{PHL}	3.3	5.9	21	5.8	23.1	ns
		5	4.2	15	4.1	16.5	
Power Dissipation Capacitance	C_{PD}§	—	66 Typ.		66 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.

$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. CP Frequency	f_{max}	5*	91	—	80	—	MHz
CP Pulse Width							
$\overline{SPE}$ HIGH (Count)	t_W	5	5.4	—	6.2	—	ns
$\overline{SPE}$ LOW (Load)	t_W	5	5.4	—	6.2	—	ns
$\overline{MR}$ Pulse Width (161)	t_W	5	5.3	—	6	—	ns
Setup Time							
Pn to CP	t_{SU}	5	4.4	—	5	—	ns
PE or TE to CP		5	5.3	—	6	—	
$\overline{SPE}$ or $\overline{MR}$ to CP (163)		5	6.6	—	7.5	—	
Hold Time							
Pn to CP	t_H	5	0	—	0	—	ns
PE or TE to CP		5	0	—	0	—	
$\overline{SPE}$ or $\overline{MR}$ to CP (163)		5	0	—	0	—	
Recovery Time							
$\overline{MR}$ to CP (161)	t_{REC}	5	5.3	—	6	—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
CP to Qn ($\overline{SPE}$ HIGH)	t_{PLH} t_{PHL}	5*	4.2	15	4.1	16.5	ns
CP to Qn ($\overline{SPE}$ LOW)		5	4.2	15	4.1	16.5	ns
CP to TC		5	4.3	15.2	4.2	16.7	ns
TE to TC		5	2.8	9.8	2.7	10.8	ns
$\overline{MR}$ to Qn (161)		5	4.2	15	4.1	16.5	ns
$\overline{MR}$ to TC (161)		5	4.2	15	4.1	16.5	ns
Power Dissipation Capacitance	C_{PD}§	—	66 Typ.		66 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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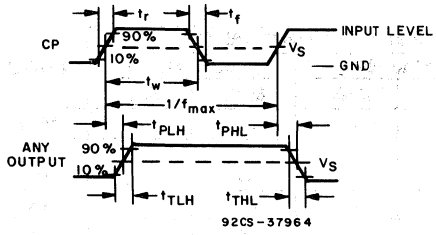
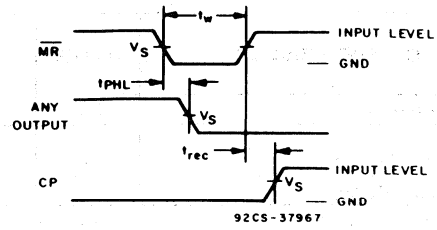
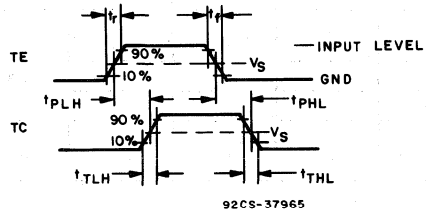
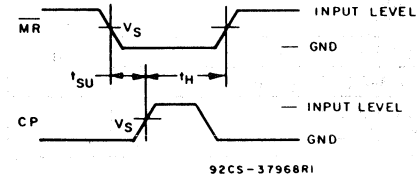
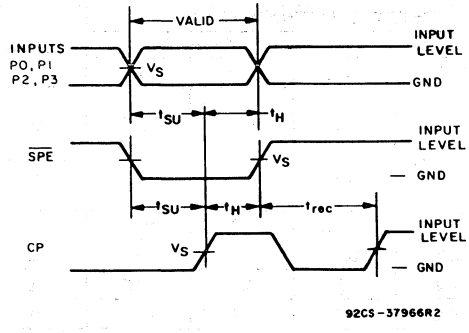
CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

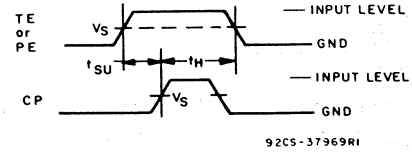


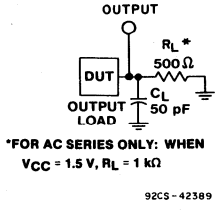












	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times, setup, hold, and recovery times, and test circuit.

Sequence illustrated in waveforms

1. **Reset outputs to zero.**
2. **Preset to binary twelve.**
3. **Count to thirteen, fourteen, fifteen, zero, one, and two.**
4. **Inhibit.**

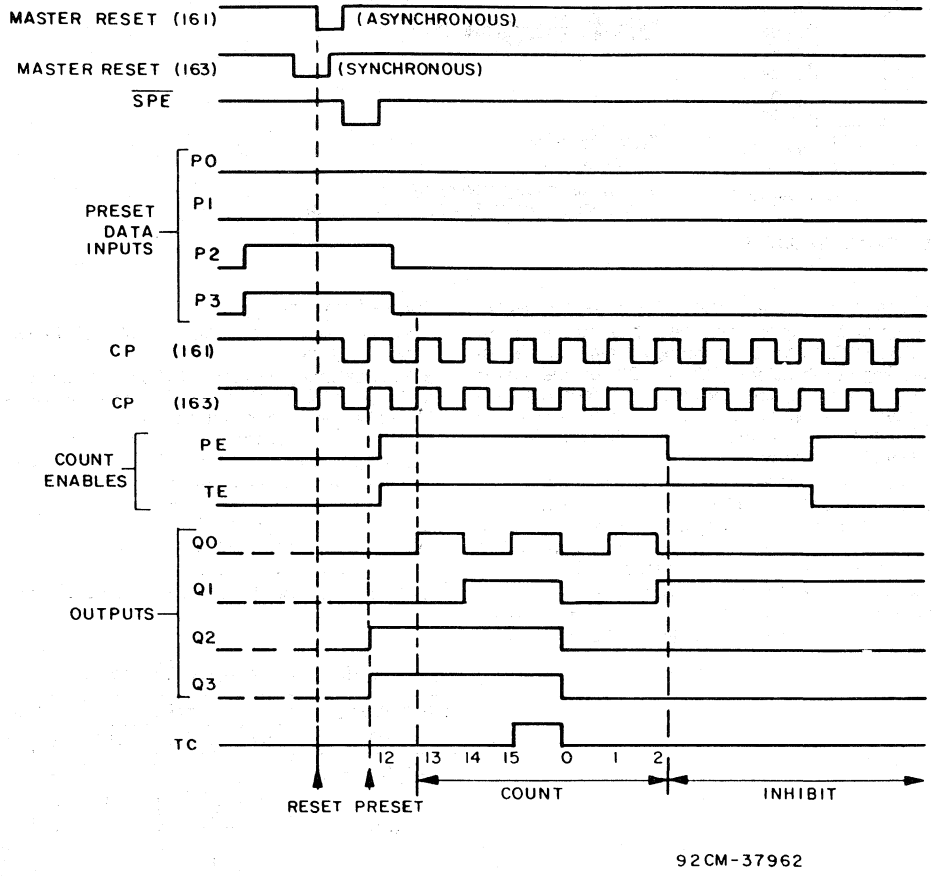
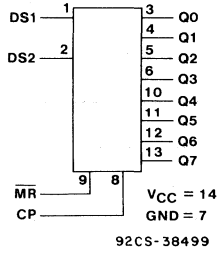


Fig. 2 - Timing diagrams for the CD54/74AC/ACT 161 and 163.

CD54/74AC164
CD54/74ACT164

Advance Information



FUNCTIONAL DIAGRAM

8-Bit Serial-In/Parallel-Out Shift Register

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 6 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC164 and CD54/74ACT164 8-bit serial-in/parallel-out shift registers with asynchronous reset use the RCA ADVANCED CMOS technology. Data is shifted on the positive edge of the clock (CP). A LOW on the Master Reset ($\overline{MR}$) pin resets the shift register and all outputs go to the LOW state regardless of the input conditions. Two Serial Data inputs (DS1 and DS2) are provided; either one can be used as a Data Enable control.

The CD74AC164 and CD74ACT164 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC164 and CD54ACT164, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	DSI	DS2	Q0	Q1 — Q7
RESET (CLEAR)	L	X	X	X	L	L — L
SHIFT	H	⎍	l	l	L	q_0 — q_6
	H	⎍	l	h	L	q_0 — q_6
	H	⎍	h	l	L	q_0 — q_6
	H	⎍	h	h	H	q_0 — q_6

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH-clock transition.
q = Lower case letters indicate the state of the reference input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
⎍ = LOW-to-HIGH clock transition.

File Number **1954**

CD54/74AC164
CD54/74ACT164

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6.0 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For $T_A = -55$ to $+100°C$ (PACKAGE TYPE E) ..... 500 mW
For $T_A = +100$ to $+125°C$ (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For $T_A = -55$ to $+70°C$ (PACKAGE TYPE M) ..... 400 mW
For $T_A = +70$ to $+125°C$ (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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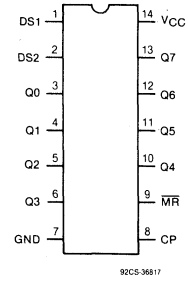

TERMINAL ASSIGNMENT

CD54/74AC164
CD54/74ACT164

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC164
CD54/74ACT164

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	--	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
DS1, DS2	0.5
$\overline{MR}$	0.74
CP	0.71

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC164
CD54/74ACT164

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}	1.5	7	—	6	—	MHz
		3.3*	62	—	54	—	
		5†	86	—	75	—	
$\overline{MR}$ Pulse Width	t_W	1.5	49	—	56	—	ns
		3.3	5.5	—	6.3	—	
		5	3.9	—	4.5	—	
CP Pulse Width	t_W	1.5	73	—	84	—	ns
		3.3	8.2	—	9.4	—	
		5	5.9	—	6.7	—	
Setup Time	t_{SU}	1.5	27	—	31	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
Hold Time	t_H	1.5	27	—	31	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
$\overline{MR}$ to CP Removal Time	t_{REM}	1.5	1	—	1	—	ns
		3.3	1	—	1	—	
		5	1	—	1	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t_{PLH} t_{PHL}	1.5	—	143	—	157	ns
		3.3*	4.5	15.9	4.4	17.5	
		5†	3.2	11.4	3.1	12.5	
$\overline{MR}$ to Qn	t_{PLH} t_{PHL}	1.5	—	158	—	174	ns
		3.3	5	17.7	4.9	19.5	
		5	3.6	12.6	3.5	13.9	
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC164
CD54/74ACT164

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{max}	5*	80	—	70	—	MHz
$\overline{MR}$ Pulse Width	t_W	5	3.9	—	4.5	—	ns
CP Pulse Width	t_W	5	6.2	—	7.1	—	ns
Setup Time	t_{SU}	5	2.2	—	2.5	—	ns
Hold Time	t_H	5	2.6	—	3	—	ns
Removal Time	t_{REM}	5	0	—	0	—	ns

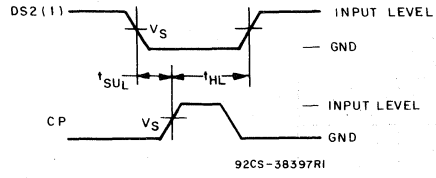
*Min. is @ 4.5 V

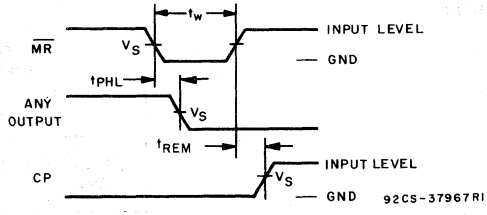
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

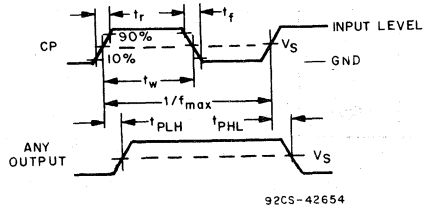
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
CP to Qn	t_{PLH}	5*	3.8	13.5	3.7	14.9	ns
$\overline{MR}$ Qn	t_{PHL}	5	4.1	14.4	4	15.8	
Power Dissipation Capacitance	C_{PD}†	—	150 Typ.		150 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

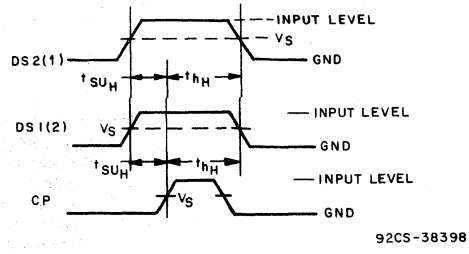
*5 V: min. is @ 5.5 V
max. is @ 4.5 V.

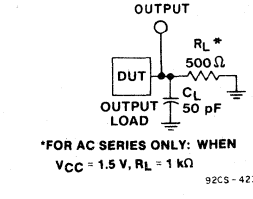
†C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$, where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.











	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times, setup and hold times, removal times, and test circuit.

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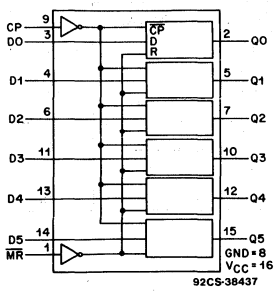
CD54/74AC174
CD54/74ACT174



FUNCTIONAL DIAGRAM

Hex D Flip-Flop with Reset

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 6.4 ns @ V_{CC} = 5V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC174 and CD54/74ACT174 are hex D flip-flops with reset that use the RCA ADVANCED CMOS technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All six flip-flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock.

The CD74AC174 and CD74ACT174 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC174 and CD54ACT174, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection — MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced Propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24 mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	⎍	H	H
H	⎍	L	L
H	L	X	Qo

H = High Level (Steady State)
L = Low Level (Steady State)
X = Irrelevant
⎍ = Transition from Low to High level
Qo = Level before the Indicated Steady-State Input conditions were established

File Number **1973**

CD54/74AC174
CD54/74ACT174

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
(For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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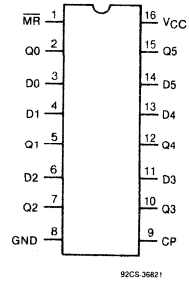

TOP VIEW
TERMINAL ASSIGNMENT

CD54/74AC174
CD54/74ACT174

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC174
CD54/74ACT174

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
Dn, $\overline{MR}$	0.5
CP	0.83

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC174
CD54/74ACT174

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t_{SU}	1.5	2	—	2	—	ns
		3.3*	2	—	2	—	
		5†	2	—	2	—	
Hold Time	t_H	1.5	33	—	38	—	ns
		3.3	3.7	—	4.2	—	
		5	2.6	—	3	—	
Removal Time $\overline{MR}$ to CP	t_{REM}	1.5	1.5	—	1.5	—	ns
		3.3	1.5	—	1.5	—	
		5	1.5	—	1.5	—	
$\overline{MR}$ Pulse Width	t_W	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	
CP Pulse Width	t_W	1.5	57	—	65	—	ns
		3.3	6.4	—	7.3	—	
		5	4.6	—	5.2	—	
CP Frequency	f_{MAX}	1.5	9	—	8	—	MHz
		3.3	77	—	68	—	
		5	108	—	95	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t_{PLH} t_{PHL}	1.5	—	154	—	169	ns
		3.3*	4.9	17.2	4.7	18.9	
		5†	3.5	12.3	3.4	13.5	
$\overline{MR}$ to Qn	t_{PLH} t_{PHL}	1.5	—	165	—	181	ns
		3.3	5.2	18.5	5.1	20.3	
		5	3.7	13.2	3.6	14.5	
Power Dissipation Capacitance	C_{PD}§	—	37 Typ.		37 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t_{SU}	5†	2	—	2	—	ns
Hold Time	t_H	5	2.2	—	2.5	—	ns
Removal Time $\overline{MR}$ to CP	t_{REM}	5	1.5	—	1.5	—	ns
$\overline{MR}$ Pulse Width	t_W	5	3.5	—	4	—	ns
CP Pulse Width	t_W	5	5.4	—	6.2	—	ns
CP Frequency	f_{MAX}	5	91	—	80	—	MHz

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t_{PLH} t_{PHL}	5†	3.6	12.6	3.5	14	ns
$\overline{MR}$ to Qn	t_{PLH} t_{PHL}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C_{PD}§	—	37 Typ.		37 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

†min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

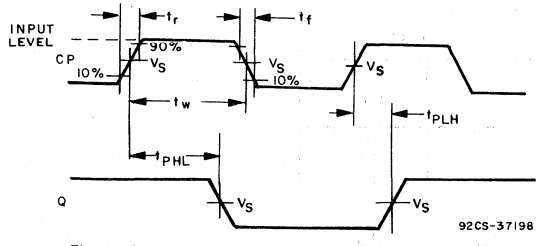

Fig. 1 - Propagation delay times and clock pulse width.

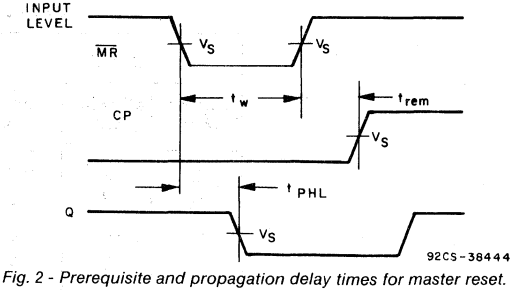

Fig. 2 - Prerequisite and propagation delay times for master reset.

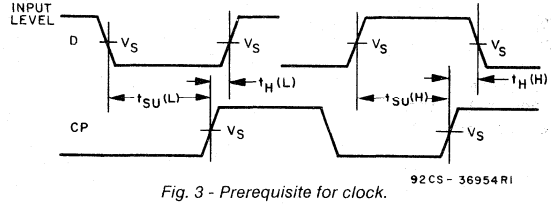

Fig. 3 - Prerequisite for clock.

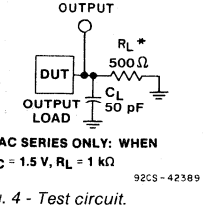

Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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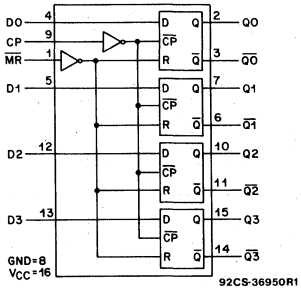
CD54/74AC175
CD54/74ACT175



FUNCTIONAL DIAGRAM

Quad D Flip-Flop with Reset

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  6.4 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA CD54/74AC175 and CD54/74ACT175 are quad D flip-flops with reset that use the RCA ADVANCED CMOS technology. Information at the D input is transferred to the Q and $\overline{Q}$ outputs on the positive-going edge of the clock pulse. All four flip-flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a LOW logic level independent of the clock.

The CD74AC175 and CD74ACT175 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC175 and CD54ACT175, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Qn	$\overline{Qn}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Qo	$\overline{Qo}$

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant
↑ = Transition from low to high level
Qo, $\overline{Qo}$ = Levels before the indicated steady-state input conditions were established

File Number **1964**

CD54/74AC175
CD54/74ACT175

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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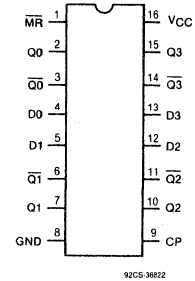

TERMINAL ASSIGNMENT

CD54/74AC175
CD54/74ACT175

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Dn	0.58
$\overline{MR}$	0.67
CP	0.92

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC175
CD54/74ACT175

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t_{SU}	1.5	2	—	2	—	ns
		3.3*	2	—	2	—	
		5†	2	—	2	—	
Hold Time	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Removal Time $\overline{MR}$ to CP	t_{REM}	1.5	1	—	1	—	ns
		3.3	1	—	1	—	
		5	1	—	1	—	
$\overline{MR}$ Pulse Width	t_W	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	
CP Pulse Width	t_W	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
CP Frequency	f_{MAX}	1.5	9	—	8	—	MHz
		3.3	81	—	71	—	
		5	114	—	100	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1.5	—	139	—	153	ns
		3.3*	4.4	15.5	4.3	17.1	
		5†	3.2	11.1	3.1	12.2	
$\overline{MR}$ to Q, $\overline{Q}$	t_{PLH} t_{PHL}	1.5	—	139	—	153	ns
		3.3	4.4	15.5	4.3	17.1	
		5	3.2	11.1	3.1	12.2	
Power Dissipation Capacitance	C_{PD}§	—	55 Typ.		55 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V.
max. is @ 3 V.

†5 V: min. is @ 5.5 V.
max. is @ 4.5 V.

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t_{SU}	5†	2	—	2	—	ns
Hold Time	t_H	5	2	—	2	—	ns
Removal Time $\overline{MR}$ to CP	t_{REM}	5	1	—	1	—	ns
$\overline{MR}$ Pulse Width	t_W	5	3.5	—	4	—	ns
CP Pulse Width	t_W	5	4.4	—	5	—	ns
CP Frequency	f_{max}	5	114	—	100	—	MHz

† min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q, $\overline{Q}$	t_{PLH} t_{PHL}	5†	3	10.5	2.9	11.5	ns
$\overline{MR}$ to Q, $\overline{Q}$		5	3.3	11.8	3.3	13	ns
Power Dissipation Capacitance	C_{PD}§	—	55 Typ.		55 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

† min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

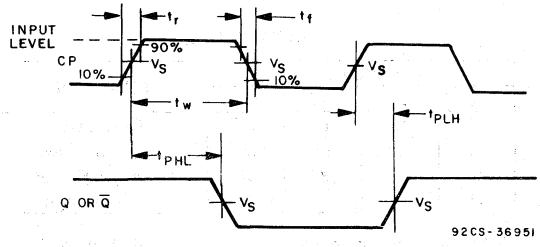


Fig. 1 - Propagation delay times and clock pulse width.

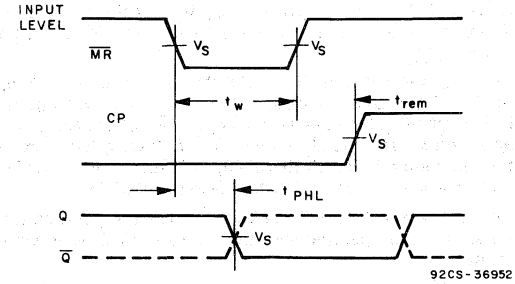


Fig. 2 - Prerequisite and propagation delay times for master reset.

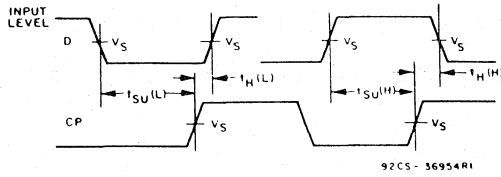


Fig. 3 - Prerequisite for clock.

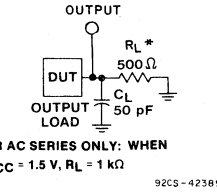
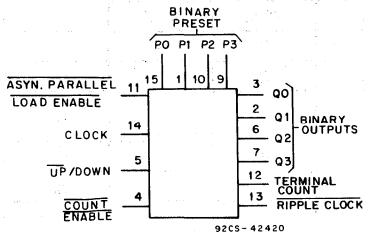


Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

CD54/74AC191
CD54/74ACT191



FUNCTIONAL DIAGRAM

Presettable Synchronous 4-Bit Binary Up/Down Counter

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  12.8 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA-CD54/74AC191 and CD54/74ACT191 asynchronously presettable binary up/down synchronous counters use the RCA ADVANCED CMOS technology. Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by setting LOW the asynchronous parallel load input ($\overline{PL}$). Counting occurs when $\overline{PL}$ is HIGH, Count Enable ($\overline{CE}$) is LOW, and the Up/Down ($\overline{U}$/D) input is either LOW for up-counting or HIGH for down-counting. The counter is incremented or decremented synchronously with the LOW-to-HIGH transition of the clock.

When an overflow or underflow of the counter occurs, the Terminal Count (TC) output, which is LOW during counting, goes HIGH and remains HIGH for one clock cycle. This output can be used for look-ahead carry in high-speed cascading (see Fig. 4). The TC output also initiates the Ripple Clock ($\overline{RC}$) output which, normally HIGH, goes LOW and remains LOW for the low-level portion of the clock pulse. These counters can be cascaded using the Ripple Count output.

The CD74AC191 and CD74ACT191 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70° C); Industrial (-40 to +85° C); and Extended Industrial/Military (-55 to +125° C).

The CD54AC191 and CD54ACT191, available in chip form (H suffix), are operable over the -55 to +125° C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS				FUNCTION
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	_/‾	Count Up
H	L	H	_/‾	Count Down
L	X	X	X	Asyn. Preset
H	H	X	X	No Change

Note:
$\overline{U}$/D or $\overline{CE}$ should be changed only when clock is high.
X = Don't care.
_/‾ = Low-to-high clock transition.

File Number **1911**

CD54/74AC191
CD54/74ACT191

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (PD):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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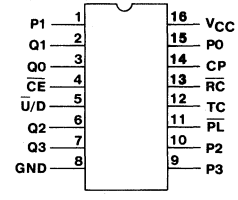

92CS-38521

TERMINAL ASSIGNMENT

CD54/74AC191
CD54/74ACT191

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5		2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C..

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
P0 — P3, $\overline{PL}$	0.75
CL, $\overline{U}$/D, $\overline{CE}$	0.85

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC191
CD54/74ACT191

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f_{max}‡	1.5	5.5	—	4.8	—	MHz
		3.3*	49	—	43	—	
		5†	68	—	60	—	
CP Pulse Width	t_W	1.5	91	—	104	—	ns
		3.3	10.5	—	11.6	—	
		5	7.3	—	8.3	—	
$\overline{PL}$ Pulse Width	t_W	1.5	66	—	75	—	ns
		3.3	7.4	—	8.4	—	
		5	5.3	—	6	—	
Recovery Time	t_{REC}	1.5	71	—	81	—	ns
		3.3	8	—	9.1	—	
		5	5.7	—	6.5	—	
Setup Time: Pn to $\overline{PL}$	t_{SU}	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	
$\overline{CE}$ to CP	t_{SU}	1.5	115	—	131	—	ns
		3.3	12.9	—	14.7	—	
		5	9.2	—	10.5	—	
$\overline{U}$/D to CP	t_{SU}	1.5	132	—	150	—	ns
		3.3	14.7	—	16.8	—	
		5	10.5	—	12	—	
Hold Time: Pn to PL	t_H	1.5	22	—	25	—	ns
		3.3	2.5	—	2.8	—	
		5	2	—	2	—	
$\overline{CE}$ to CP	t_H	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	
$\overline{U}$/D to CP	t_H	1.5	0	—	0	—	ns
		3.3	0	—	0	—	
		5	0	—	0	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

‡Applies to non-cascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enable ($\overline{CE}$)-to-clock set-up times, and count enable ($\overline{CE}$)-to-clock hold times determine max. clock frequency. For example, with these AC devices @ 85° C and V_{CC} = 5 V:

$$f_{max}\,(CP) = \frac{1}{\text{CP-to-TC prop. delay} + \overline{CE}\text{-to-CP setup} + \overline{CE}\text{-to-CP Hold}} = \frac{1}{18.2 + 9.2 + 0} \approx 36\ \text{MHz}$$

SWITCHING CHARACTERISTICS: AC Series; t_r t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
$\overline{PL}$ to Qn	t_{PLH}	1.5	—	171	—	188	
	t_{PHL}	3.3*	5.4	19.1	5.3	21	ns
		5†	3.9	13.6	3.8	15	
Pn to Qn	t_{PLH}	1.5	—	173	—	190	
	t_{PHL}	3.3	5.4	19.4	5.3	21.3	ns
		5	3.9	13.8	3.8	15.2	
CP to Qn	t_{PLH}	1.5	—	182	—	200	
	t_{PHL}	3.3	5.8	20.4	5.6	22.4	ns
		5	4.1	14.5	4	16	
CP to $\overline{RC}$	t_{PLH}	1.5	—	136	—	150	
	t_{PHL}	3.3	4.3	15.3	4.2	16.8	ns
		5	3.1	11	3	12	
CP to TC	t_{PLH}	1.5	—	227	—	250	
	t_{PHL}	3.3	7.2	25.5	7	28	ns
		5	5.2	18.2	5	20	
$\overline{U}$/D to $\overline{RC}$	t_{PLH}	1.5	—	246	—	271	
	t_{PHL}	3.3	7.8	27.6	7.6	30.4	ns
		5	5.6	19.7	5.4	21.7	
$\overline{U}$/D to TC	t_{PLH}	1.5	—	160	—	176	
	t_{PHL}	3.3	5.1	17.9	4.9	19.7	ns
		5	3.6	12.8	3.5	14.1	
$\overline{CE}$ to $\overline{RC}$	t_{PLH}	1.5	—	137	—	151	
	t_{PHL}	3.3	4.4	15.4	4.2	16.9	ns
		5	3.1	11	3	12.1	
Power Dissipation Capacitance	C_{PD}§	—	96 Typ.		96 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD}V_{CC}^2 f_i + (C_L V_{CC}^2 f_o)$ where fi = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC191
CD54/74ACT191

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f_{max}‡	5†	68	—	60	—	MHz
CP Pulse Width	t_W	5	7.3	—	8.3	—	ns
$\overline{PL}$ Pulse Width	t_W	5	5.3	—	6	—	ns
Recovery Time	t_{REC}	5	5.7	—	6.5	—	ns
Setup Time:							
Pn to $\overline{PL}$	t_{SU}	5	3.5	—	4	—	ns
$\overline{CE}$ to CP		5	9.2	—	10.5	—	
$\overline{U}$/D to CP		5	10.5	—	12	—	
Hold Time:							
Pn to $\overline{PL}$	t_H	5	2	—	2	—	ns
$\overline{CE}$ to CP		5	0	—	0	—	
$\overline{U}$/D to CP		5	0	—	0	—	

†min. is @ 4.5 V

‡Applies to non-cascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enable ($\overline{CE}$)-to-clock set-up times, and count enable ($\overline{CE}$)-to-clock hold times determine max. clock frequency. For example, with these ACT devices @ 85°C:

$$f_{max}\,(CP) = \frac{1}{\text{CP-to-TC prop. delay} + \overline{CE}\text{-to-CP setup} + \overline{CE}\text{-to-CP Hold}} = \frac{1}{18.2 + 9.2 + 0} \approx 36\ \text{MHz}$$

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
$\overline{PL}$ to Qn		5†	4.2	14.8	4.1	16.3	ns
Pn to Qn		5	3.9	13.8	3.8	15.2	
CP to Qn		5	4.1	14.5	4	16	
CP to $\overline{RC}$	t_{PLH}	5	3.1	10.9	3	12	
CP to TC	t_{PHL}	5	5.2	18.2	5	20	
$\overline{U}$/D to $\overline{RC}$		5	5.6	19.7	5.4	21.7	
$\overline{U}$/D to TC		5	3.8	13.5	3.7	14.9	
$\overline{CE}$ to $\overline{RC}$		5	3.3	11.5	3.2	12.7	
Power Dissipation Capacitance	C_{PD}§	—	96 Typ.		96 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

†Min. is @ 5.5 V
Max. is @ 4.5 V.

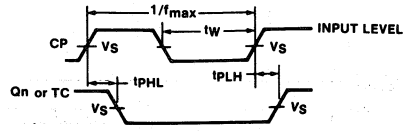
§C_{PD} is used to determine the dynamic power consumption, per package.

$P_D = C_{PD}V_{CC}^2 f_i + (C_L V_{CC}^2 f_o) + V_{CC}\,\Delta I_{CC}$ where fi = input frequency

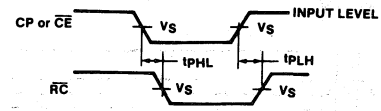
f_o = output frequency

C_L = output load capacitance

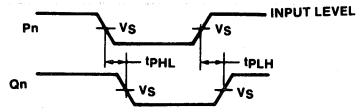
V_{CC} = supply voltage.



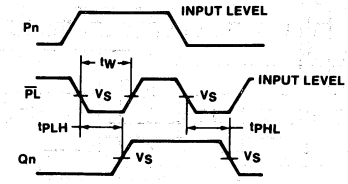
Waveform 1



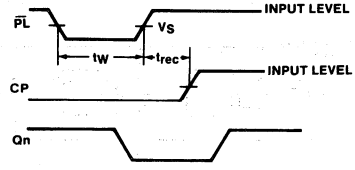
Waveform 2



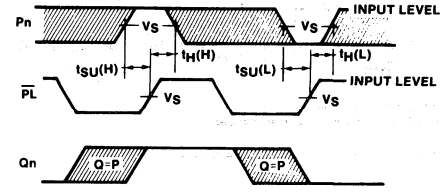
Waveform 3



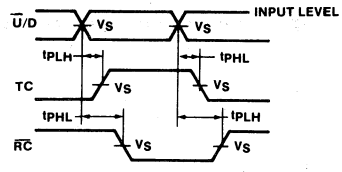
Waveform 4



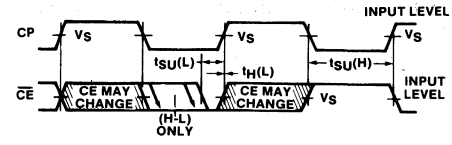
Waveform 5



Waveform 6



Waveform 7



Waveform 8

The shaded areas indicate when the input is permitted to change for predictable output performance

92CL-38403R3

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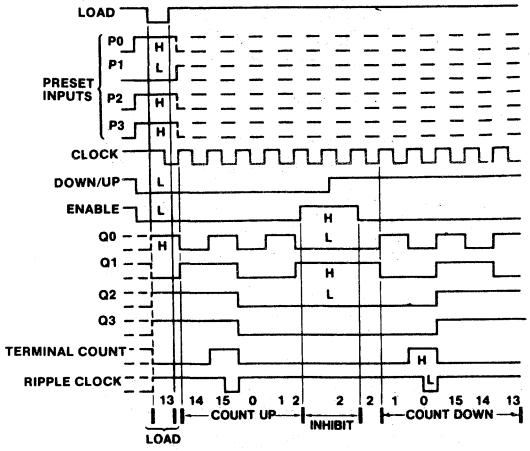
	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Transition, propagation delay, setup and hold, and removal times.

CD54/74AC191
CD54/74ACT191

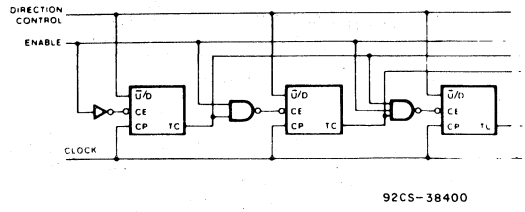
TIMING DIAGRAM



Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

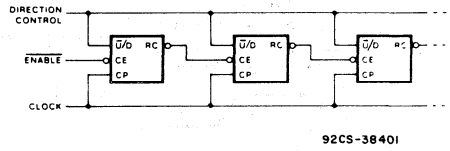
92CM-38402

Fig. 2 - AC191 decode counters typical load, count, and inhibit sequences.



92CS-38400

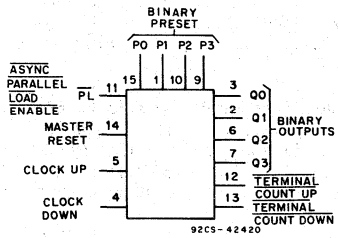
Fig. 3 - Synchronous n-stage counter with parallel gated TC/$\overline{RC}$.



92CS-38401

Fig. 4 - Synchronous n-stage counter using ripple TC/$\overline{RC}$.

CD54/74AC193
CD54/74ACT193



FUNCTIONAL DIAGRAM

Presettable Synchronous 4-Bit Binary Up/Down Counter with Reset

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  11.2 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA-CD54/74AC193 and CD54/74ACT193 are up/down binary counters with separate up/down clocks. These devices use the RCA ADVANCED CMOS technology. Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input ($\overline{PL}$). The counter is incremented on the LOW-to-HIGH transition of the Clock-Up input (and a HIGH level on the Clock-Down input) and decremented on the LOW-to-HIGH transition of the Clock-Down input (and a HIGH level on the Clock-Up input). A HIGH level on the Reset input overrides any other input to clear the counter to its zero state. The $\overline{TCU}$ (carry) output goes LOW half a clock period before the zero count is reached and returns to a HIGH level at the zero count. The $\overline{TCD}$ (borrow) output in the count down mode likewise goes LOW half a clock period before the maximum count (15 counts) and returns to HIGH at the maximum count. Cascading is effected by connecting the $\overline{TCU}$ and $\overline{TCD}$ outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

The CD74AC/ACT193 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC193 and CD54ACT193, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST®* ICs
  - Drives 50-ohm transmission lines

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TRUTH TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FUNCTION
⎍	H	L	H	Count Up
H	⎍	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

H = High level
L = Low level
⎍ = Low-to-high transition
X = Don't care

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File Number **1947**

CD54/74AC193
CD54/74ACT193

MAXIMUM RATINGS, *Absolute-Maximum Values:*

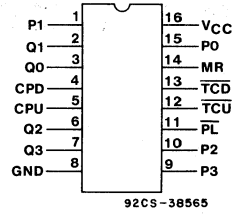
DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.



TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC193
CD54/74ACT193

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
P0 - P3, $\overline{PL}$	0.75
MR, CPU, CPD	0.85

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width		1.5	64	—	73	—	
CPD	t_w	3.3*	7.1	—	8.1	—	ns
		5†	5.1	—	5.8	—	
$\overline{CPU}$		1.5	73	—	83	—	
	t_w	3.3	8.1	—	9.2	—	ns
		5	5.8	—	6.6	—	
$\overline{PL}$ Pulse Width		1.5	66	—	75	—	
	t_w	3.3	7.4	—	8.4	—	ns
		5	5.3	—	6	—	
MR Pulse Width		1.5	55	—	63	—	
	t_w	3.3	6.1	—	7	—	ns
		5	4.4	—	5	—	
Recovery Time		1.5	55	—	63	—	
$\overline{PL}$ to CPU or CPD	t_{REC}	3.3	6.1	—	7	—	ns
		5	4.4	—	5	—	
Recovery Time		1.5	1	—	1	—	
MR to CPU, CPD	t_{REC}	3.3	1	—	1	—	ns
		5	1	—	1	—	
Setup Time		1.5	44	—	50	—	
Pn to $\overline{PL}$	t_{SU}	3.3	4.9	—	5.6	—	ns
		5	3.5	—	4	—	
Hold Time		1.5	2	—	2	—	
Pn to $\overline{PL}$	t_H	3.3	2	—	2	—	ns
		5	2	—	2	—	
Max. Frequency		1.5	6.8	—	6	—	
CPU		3.3	62	—	54	—	MHz
	f_{max}	5	86	—	75	—	
$\overline{CPD}$		1.5	7.8	—	6.8	—	
		3.3	70	—	61	—	MHz
		5	97	—	85	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

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CD54/74AC193
CD54/74ACT193

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
$\overline{PL}$ to Qn	t_{PLH}	1.5	—	171	—	188	ns
	t_{PHL}	3.3*	5.4	19.1	5.3	21	
		5†	3.9	13.6	3.8	15	
CPU to Qn	t_{PLH}	1.5	—	159	—	175	ns
CPD to Qn	t_{PHL}	3.3	5	17.8	4.9	19.6	
		5	3.6	12.7	3.5	14	
CPU to $\overline{TCU}$	t_{PLH}	1.5	—	127	—	140	ns
CPD to $\overline{TCD}$	t_{PHL}	3.3	4	14.3	3.9	15.7	
		5	2.9	10.2	2.8	11.2	
MR to Qn	t_{PLH}	1.5	—	182	—	200	ns
	t_{PHL}	3.3	5.8	20.4	5.6	22.4	
		5	4.1	14.5	4	16	
MR to $\overline{TCU}$	t_{PLH}	1.5	—	171	—	188	ns
	t_{PHL}	3.3	5.5	19.1	5.3	21	
		5	3.9	13.6	3.8	15	
MR to $\overline{TCD}$	t_{PLH}	1.5	—	207	—	228	ns
	t_{PHL}	3.3	6.6	23.2	6.4	25.5	
		5	4.7	16.5	4.6	18.2	
Pn to Qn	t_{PLH}	1.5	—	187	—	206	ns
	t_{PHL}	3.3	5.9	21	5.8	23.1	
		5	4.2	15	4.1	16.5	
Power Dissipation Capacitance	C_{PD}§	—	95 Typ.		95 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_O = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width: CPU	t_w	5†	6.8	—	7.7	—	ns
CPD			5.8	—	6.6	—	
$\overline{PL}$ Pulse Width	t_w	5	6.6	—	7.5	—	ns
MR Pulse Width	t_w	5	4.4	—	5	—	ns
Recovery Time: $\overline{PL}$ to CPU or CPD	t_{REC}	5	5.7	—	6.5	—	ns
MR to CPU, CPD			1	—	1	—	
Setup Time Pn to $\overline{PL}$	t_{SU}	5	4.7	—	5.4	—	ns
Hold Time Pn to $\overline{PL}$	t_H	5	2	—	2	—	ns
Max. Frequency: CPU	f_{max}	5	74	—	65	—	MHz
CPD			86	—	75	—	

†5V min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: $\overline{PL}$ to Qn	t_{PLH} t_{PHL}	5†	3.9	13.6	3.8	15	ns
CPU to Qn		5	3.6	12.7	3.5	14	
CPD to Qn		5	3.6	12.7	3.5	14	
CPU to $\overline{TCU}$		5	2.9	10.2	2.8	11.2	
CPD to $\overline{TCD}$		5	2.9	10.2	2.8	11.2	
MR to Qn		5	4.1	14.5	4	16	
MR to $\overline{TCU}$		5	3.9	13.6	3.8	15	
MR to $\overline{TCD}$		5	4.7	16.5	4.6	18.2	
Pn to Qn		5	4.2	15	4.1	16.5	
Power Dissipation Capacitance	C_{PD}§	—	95 Typ.		95 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

†5V: min. is @ 5.5 V
max. is @ 4.5 V.

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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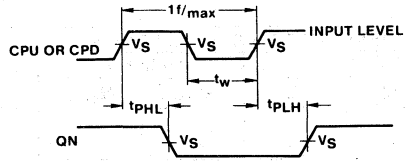
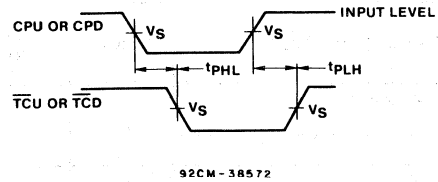
CD54/74AC193
CD54/74ACT193



(a) *Clock to output delays and clock pulse width.*



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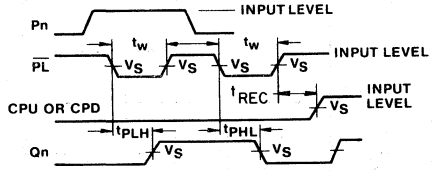
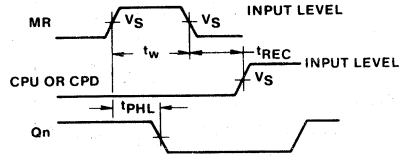
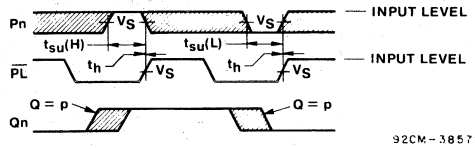
(b) *Clock to terminal count delays.*



(c) *Parallel load pulse width, parallel load to output delays, and parallel load to clock recovery time.*



(d) *Master reset pulse width, master reset to output delay and master reset to clock recovery time.*



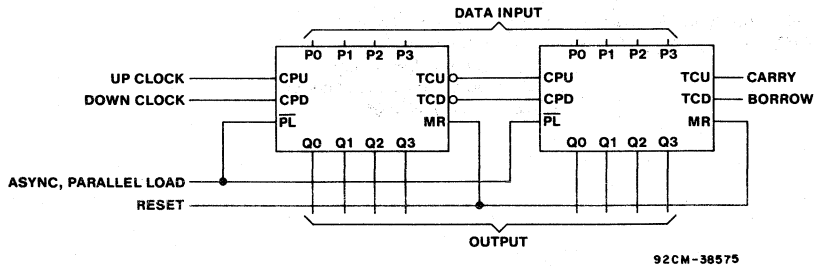
92CM-38571R2

(e) *Setup and hold times data to parallel load (PL).*

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - AC waveforms.

APPLICATION



92CM-38575

CASCADED UP/DOWN COUNTER WITH PARALLEL LOAD

Sequences:
(1) Reset outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, terminal count up, zero, one and two.
(4) Count down to one, zero, terminal count down, fifteen, fourteen and thirteen.

Note 1: Master reset overrides load data and clock inputs
Note 2: When counting up, clock-down input must be high; when counting down, clock-up input must be high.

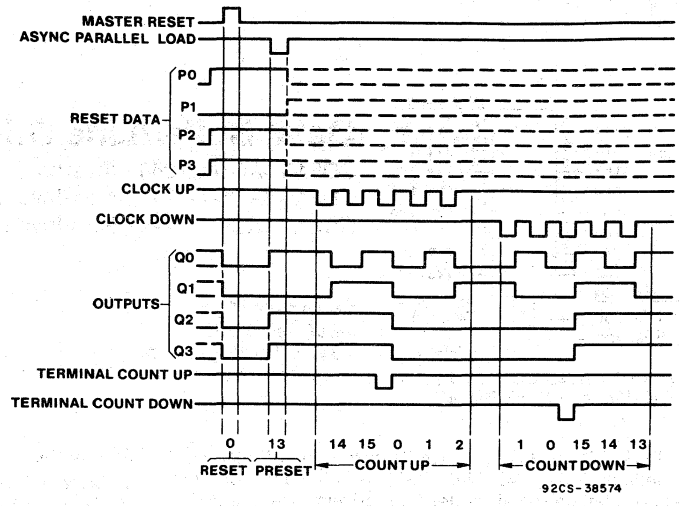


Fig. 2 - Timing diagram.

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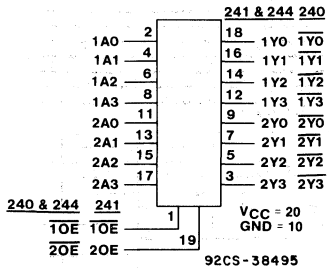
CD54/74AC240/241/244
CD54/74ACT240/241/244

Advance Information



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

Octal Buffer/Line Drivers, 3-State

CD54/74AC/ACT240 - Inverting
CD54/74AC/ACT241 - Non-Inverting
CD54/74AC/ACT244 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.6 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC240, CD54/74AC241, and CD54/74AC-244 and the CD54/74ACT240, CD54/74ACT241, and CD54/74-ACT244 3-state octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT240 and CD54/74AC/ACT244 have active-LOW output enables ($\overline{1OE}$, $\overline{2OE}$). The CD54/74AC/ACT241 has one active-LOW (1OE) and one active-HIGH (2OE) output enable.

The CD74AC240, CD74AC241, and CD74AC244 and the CD74ACT240, CD74ACT241, and CD74ACT244 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC240, CD54AC241, and CD54AC244 and the CD54ACT240, CD54ACT241, and CD54ACT244, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLES

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	H
L	H	L
H	X	Z

(AC/ACT240)

INPUTS		OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(AC/ACT244)

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{1OE}$	1A	1Y	2OE	2A	2Y
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

(AC/ACT241)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

File Number **1856**

CD54/74AC240/241/244
CD54/74ACT240/241/244

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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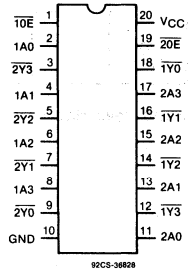
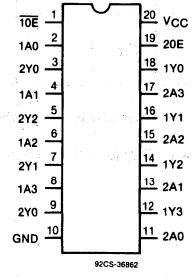
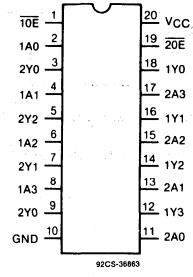


CD54/74AC, ACT240 TYPES TERMINAL ASSIGNMENT



CD54/74AC, ACT241 TYPES TERMINAL ASSIGNMENT



CD54/74AC, ACT244 TYPES TERMINAL ASSIGNMENT

CD54/74AC240/241/244
CD54/74ACT240/241/244

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC240/241/244
CD54/74ACT240/241/244

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLES

CD54/74ACT240	
INPUT	UNIT LOADS*
nA0 - A3	1.42
$\overline{10E}$	0.83
$\overline{20E}$	0.83

CD54/74ACT241	
INPUT	UNIT LOADS*
nA0 - A3	0.5
$\overline{10E}$	0.83
20E	1.67

CD54/74ACT244	
INPUT	UNIT LOADS*
nA0 - A3	0.5
$\overline{10E}$	0.83
$\overline{20E}$	0.83

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC240/241/244
CD54/74ACT240/241/244

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs AC240	t_{PLH} t_{PHL}	1.5	—	82	—	90	ns
		3.3*	2.6	9.2	2.5	10.1	
		5†	1.9	6.5	1.8	7.2	
AC241, 244	t_{PLH} t_{PHL}	1.5	—	93	—	103	ns
		3.3	3	10.5	2.9	11.5	
		5	2.2	7.5	2.1	8.2	
Output Enable Times	t_{PZL} t_{PZH}	1.5	—	136	—	150	ns
		3.3	4.6	16.4	4.5	18	
		5	3.1	10.9	3	12	
Output Disable Times	t_{PLZ} t_{PHZ}	1.5	—	136	—	150	ns
		3.3	3.9	13.6	3.8	15	
		5	3.1	10.9	3	12	
Power Dissipation Capacitance AC240	C_{PD}§	—	65 Typ.		65 Typ.		pF
AC241, 244		—	71 Typ.		71 Typ.		
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Outputs ACT240	t_{PLH} t_{PHL}	5†	2.3	7.8	2.2	8.6	ns
ACT241, 244	t_{PLH} t_{PHL}	5	2.5	8.7	2.4	9.6	ns
Output Enable Times	t_{PZL} t_{PZH}	5	3.5	12.2	3.4	13.4	ns
Output Disable Times	t_{PLZ} t_{PHZ}	5	3.5	12.2	3.4	13.4	ns
Power Dissipation Capacitance ACT240	C_{PD}§	—	65 Typ.		65 Typ.		pF
ACT241, 244		—	71 Typ.		71 Typ.		
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

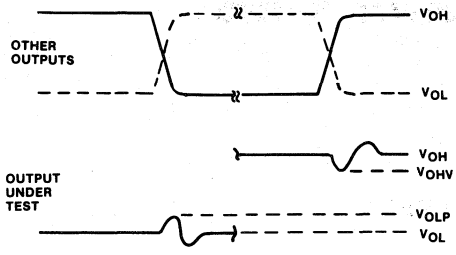
*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

‡C_{PD} is used to determine the dynamic power consumption, per package.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC240/241/244
CD54/74ACT240/241/244

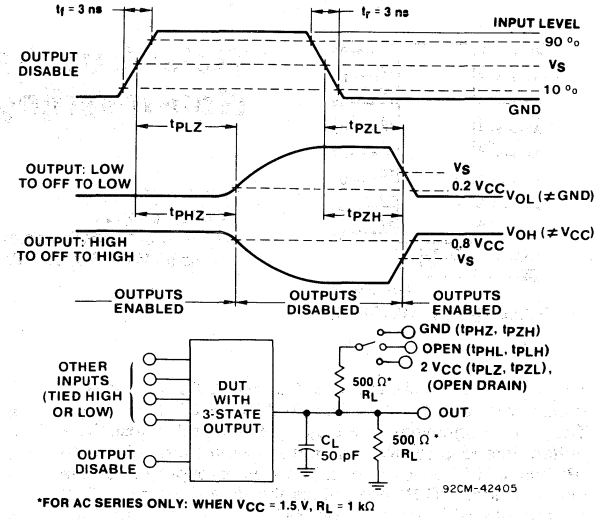
PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

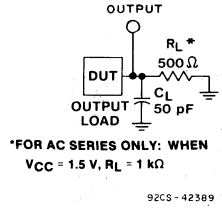
92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 2 - Three-state propagation delay times and test circuit.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

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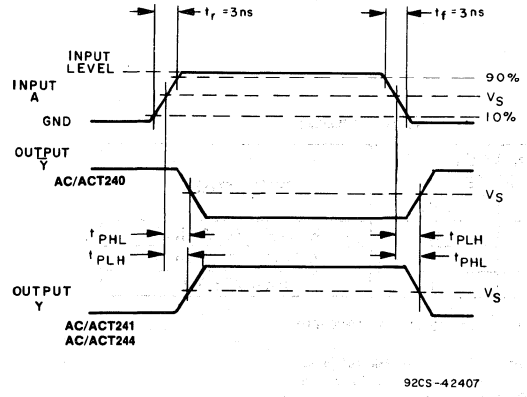

Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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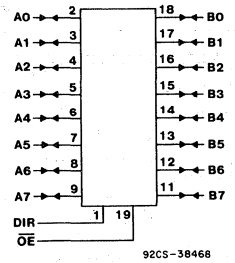
CD54/74AC245
CD54/74ACT245



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver, 3-State, Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  4 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA CD54/74AC245 and CD54/74ACT245 octal-bus transceivers use the RCA ADVANCED CMOS technology. They are non-inverting 3-state bidirectional transceiver-buffers intended for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus. The logic level present on the direction input (DIR) determines the data direction. When the output enable input ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state.

The CD74AC245 and CD74ACT245 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC245 and CD54ACT245, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

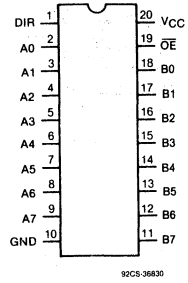
®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B DATA TO A BUS
L	H	A DATA TO B BUS
H	X	ISOLATION

H = high level, L = low level, X = irrelevant

To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10KΩ to 1MΩ resistors.



TERMINAL ASSIGNMENT

File Number **1907**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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CD54/74AC245
CD54/74ACT245

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
An, Bn	0.83
$\overline{OE}$	0.64
DIR	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC245
CD54/74ACT245

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	t_{PLH} t_{PHL}	1.5	—	96	—	106	ns
		3.3*	3.2	10.8	3	11.9	
		5†	2.2	7.7	2.1	8.5	
Output Disable to Output	t_{PLZ} t_{PHZ}	1.5	—	159	—	175	ns
		3.3	4.7	15.9	4.4	17.5	
		5	3.7	12.7	3.5	14	
Output Enable to Output	t_{PZL} t_{PZH}	1.5	—	159	—	175	ns
		3.3	5.6	19	5.3	21	
		5	3.7	12.7	3.5	14	
Power Dissipation Capacitance	C_{PD}§	—	57 Typ.		57 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

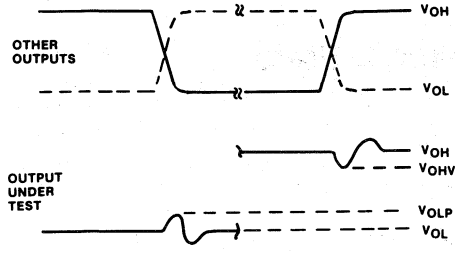
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	t_{PLH} t_{PHL}	5†	2.7	9.1	2.5	10	ns
Output Disable to Output	t_{PLZ} t_{PHZ}	5	3.7	12.7	3.5	14	ns
Output Enable to Output	t_{PZH} t_{PZL}	5	3.8	13.1	3.6	14.4	ns
Power Dissipation Capacitance	C_{PD}§	—	57 Typ.		57 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per channel.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.

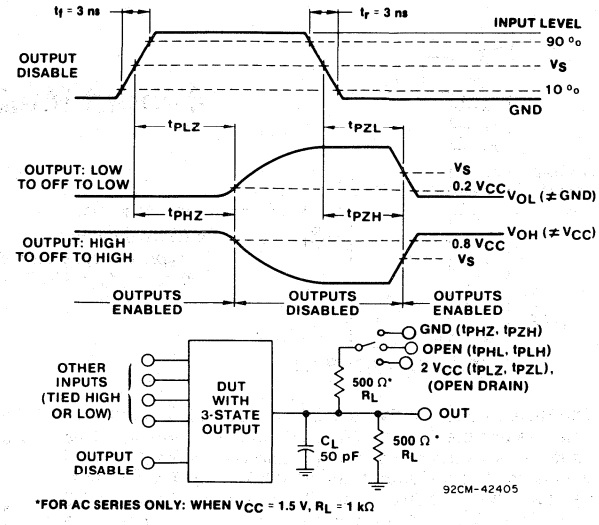
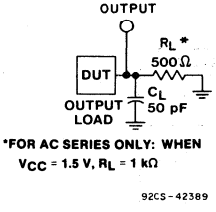


Fig. 2 - Three-state propagation delay times and test circuit.



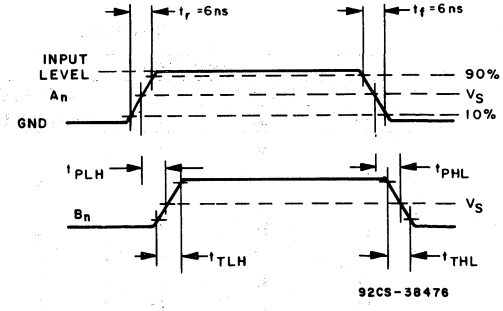
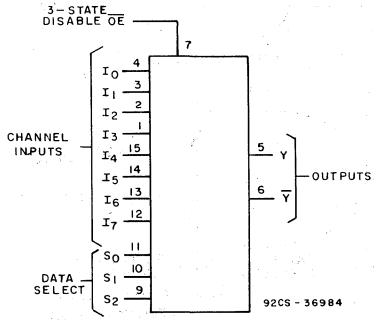


Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

CD54/74AC251
CD54/74ACT251

Advance Information



FUNCTIONAL DIAGRAM

8-Input Multiplexer, 3-State

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 6 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC251 and CD54/74ACT251 8-input multiplexers use the RCA ADVANCED CMOS technology. This multiplexer features both true (Y) and complement ($\overline{Y}$) outputs as well as an Output Enable ($\overline{OE}$) input. The $\overline{OE}$ must be at a LOW logic level to enable this device. When the $\overline{OE}$ input is HIGH, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and $\overline{Y}$ outputs.

The CD74AC251 and CD74ACT251 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC251 and CD54ACT251, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

**FAST is a Registered Trademark of Fairchild Semiconductor Corp.*

TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			OUTPUT		
S2	S1	S0	ENABLE $\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	$\overline{Z}$
L	L	L	L	I_0	$\overline{I_0}$
L	L	H	L	I_1	$\overline{I_1}$
L	H	L	L	I_2	$\overline{I_2}$
L	H	H	L	I_3	$\overline{I_3}$
H	L	L	L	I_4	$\overline{I_4}$
H	L	H	L	I_5	$\overline{I_5}$
H	H	L	L	I_6	$\overline{I_6}$
H	H	H	L	I_7	$\overline{I_7}$

H = High logic level
L = Low logic level
X = Irrelevant
Z = High impedance (off)
I_0, I_1 . . . I_7 = The level of the respective input

File Number **1981**

CD54/74AC251
CD54/74ACT251

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
(For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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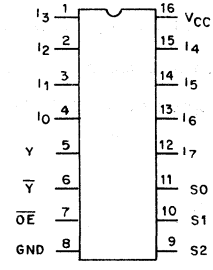

92CS-36831

TERMINAL ASSIGNMENT

CD54/74AC251
CD54/74ACT251

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85° C, 75 ohms at +125° C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
S0, S1, S3	1
OE	1
I_0 - I_7	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC251
CD54/74ACT251

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Y Output	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 4.9 3.5	153 17.2 12.3	— 4.7 3.4	169 18.9 13.5	ns
Data to $\overline{Y}$ Output	t_{PLH} t_{PHL}	1.5 3.3 5	— 5.4 3.8	169 19 13.5	— 5.2 3.7	186 20.9 14.9	ns
Select to Y Output	t_{PLH} t_{PHL}	1.5 3.3 5	— 6.6 4.7	207 23.2 16.5	— 6.4 4.6	228 25.5 18.2	ns
Select to $\overline{Y}$ Output	t_{PLH} t_{PHL}	1.5 3.3 5	— 7.1 5.1	223 24.9 17.8	— 6.9 4.9	245 27.4 19.6	ns
Output Enable and Output Disable to Output	t_{PZH} t_{PZL} t_{PHZ} t_{PLZ}	1.5 3.3 5	— 5.2 3.5	155 18.7 12.3	— 5.1 3.4	169 20.3 13.5	ns
Power Dissipation Capacitance	C_{PD}§	—	120 Typ.		120 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Y Output	t_{PLH} t_{PHL}	5†	3.5	12.3	3.4	13.5	ns
Data to $\overline{Y}$ Output	t_{PLH} t_{PHL}	5	3.8	13.5	3.7	14.9	ns
Select to Y Output	t_{PLH} t_{PHL}	5	4.7	16.5	4.6	18.2	ns
Select to $\overline{Y}$ Output	t_{PLH} t_{PHL}	5	5.1	17.8	4.9	19.6	ns
Output Enable and Output Disable to Output	t_{PZH} t_{PZL} t_{PHZ} t_{PLZ}	5	3.5	12.3	3.4	13.5	ns
Power Dissipation Capacitance	C_{PD}§	—	120 Typ.		120 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

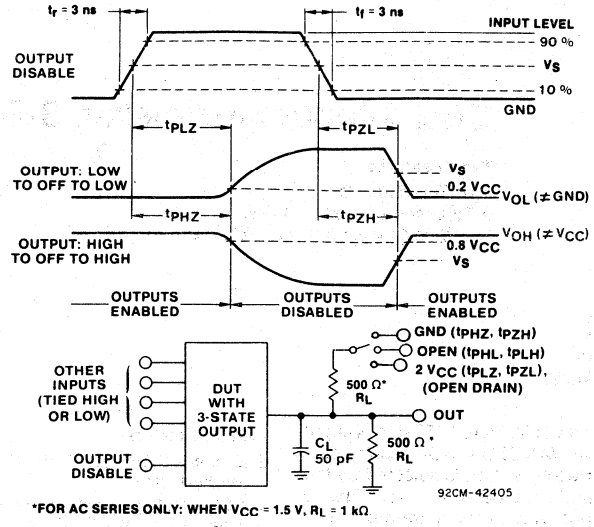


Fig. 1 - Three-state propagation delay times and test circuit.

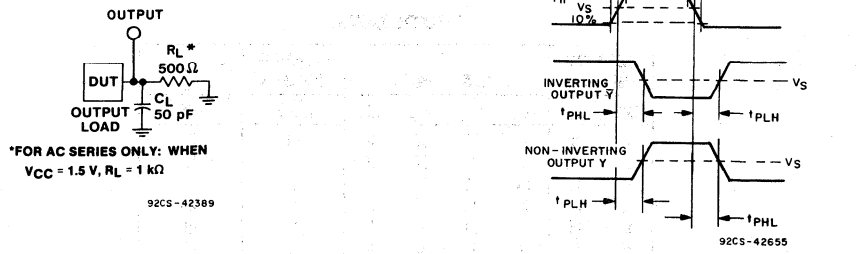
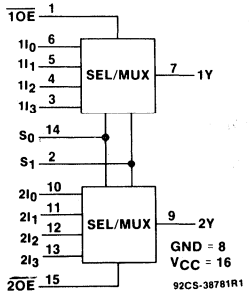


Fig. 2 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

CD54/74AC253
CD54/74ACT253

Advance Information



FUNCTIONAL DIAGRAM

Dual 4-Input Multiplexer, 3-State

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 6.3 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC253 and CD54/74ACT253 dual 4-input multiplexers use the RCA ADVANCED CMOS technology. One of the four sources for each section is selected by the common Select inputs, S0 and S1. When the Output Enable ($\overline{1OE}$ or $\overline{2OE}$) is HIGH, the output is in the high-impedance state.

The CD74AC253 and CD74ACT253 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC253 and CD54ACT253, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				ENABLE INPUTS	OUTPUT
S1	S0	nI_0	nI_1	nI_2	nI_3	$\overline{nOE}$	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs S1 and S0 are common to both sections.
H = High level
L = Low level
X = Don't care
Z = High impedance

File Number **1985**

CD54/74AC253
CD54/74ACT253

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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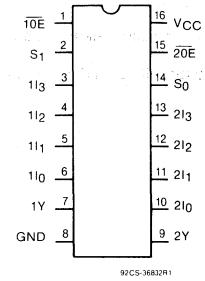

TERMINAL ASSIGNMENT

CD54/74AC253
CD54/74ACT253

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC253
CD54/74ACT253

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
S0, S1, nI_0, nI_1	1
$\overline{nOE}$	0.83

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC253
CD54/74ACT253

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: S0, S1, to Y	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 7.2 5.2	227 25 18.2	— 7 5	250 28 20	ns
nI to Y	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.8 3.4	151 16.9 12.1	— 4.7 3.3	166 18.6 13.3	ns
Output Enable, Output Disable to Y	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	1.5 3.3 5	— 4.5 3	131 15.7 10.5	— 4.3 2.9	144 17.3 11.5	ns
Power Dissipation Capacitance	C_{PD}§	—	107 Typ.		107 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: S0, S1, to Y	t_{PLH} t_{PHL}	5†	5.7	20	5.5	22	ns
nI to Y	t_{PLH} t_{PHL}	5	4.6	16.4	4.5	18	ns
Output Enable, Output Disable to Y	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.2	11.5	3.2	12.6	ns
Power Dissipation Capacitance	C_{PD}§	—	107 Typ.		107 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

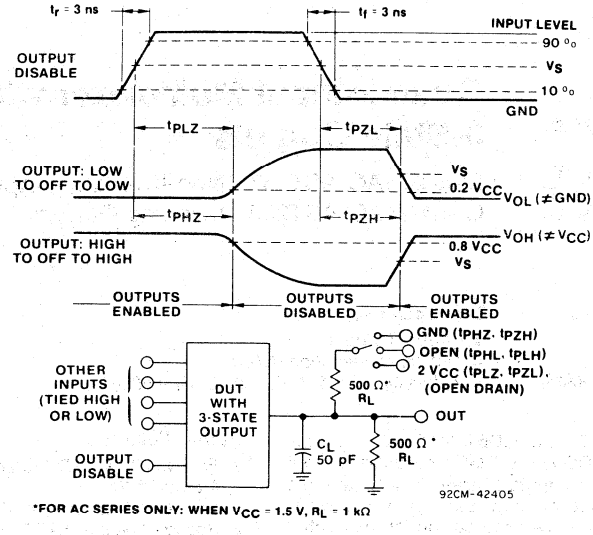

Fig. 1 - Three-state propagation delay waveforms and test circuit.

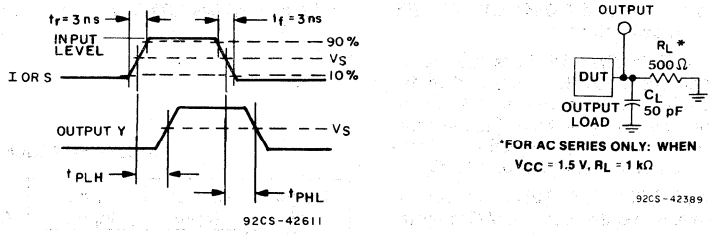

Fig. 2 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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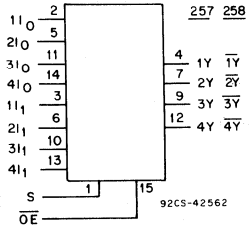
CD54/74AC257, CD54/74AC258
CD54/74ACT257, CD54/74ACT258

Advance Information



FUNCTIONAL DIAGRAM

Quad 2-Input Multiplexer with 3-State Outputs

CD54/74AC/ACT257 - Non-Inverting Outputs
CD54/74AC/ACT258 - Inverting Outputs

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  4.4 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA-CD54/74AC257 and CD54/74AC258 and the CD54/74ACT257 and CD54/74ACT258 are quad 2-input multiplexers with 3-state outputs. These devices use the RCA ADVANCED CMOS technology. Each of these devices selects four bits of data from two sources under the control of a common Select input (S). The Output Enable ($\overline{OE}$) is active LOW. When $\overline{OE}$ is HIGH, all of the outputs (Y or $\overline{Y}$) are in the high-impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the CD54/74AC/ACT257 and CD54/74AC/ACT258. The state of the Select input determines the particular register from which the data comes. The CD54/74AC/ACT257 and CD54/74AC/ACT258 can also be used as function generators.

The CD74AC/ACT257 and CD74AC/ACT258 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT257 and CD54AC/ACT258, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		257 Outputs	258 Outputs
$\overline{OE}$	S	I_0	I_1	Y	$\overline{Y}$
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High level voltage
L = Low level voltage
Z = High impedance (off) state.
X = Don't care

File Number **1955**

CD54/74AC257, CD54/74AC258
CD54/74ACT257, CD54/74ACT258

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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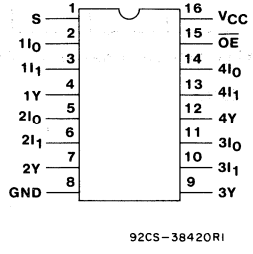
TERMINAL ASSIGNMENT DIAGRAMS



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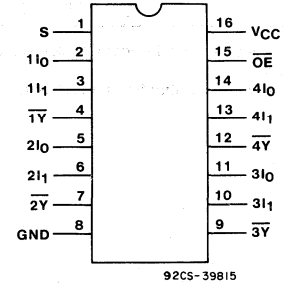
CD54/74AC/ACT257



92CS-39815

CD54/74AC/ACT258

CD54/74AC257, CD54/74AC258
CD54/74ACT257, CD54/74ACT258

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85° C, 75 ohms at +125° C.

CD54/74AC257, CD54/74AC258
CD54/74ACT257, CD54/74ACT258

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Data	0.83
S	1.27
$\overline{OE}$	1.27

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC257, CD54/74AC258
CD54/74ACT257, CD54/74ACT258

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				-40 to +85		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays: I_n to Y	257	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 3.3 2.4	106 11.8 8.5	— 3.3 2.3	117 13 9.3	ns
S to Y	257	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.8 3.5	153 17.1 12.2	— 4.7 3.4	168 18.8 13.4	ns
$\overline{OE}$ to Y	257	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	1.5 3.3 5	— 5.3 3.8	167 18.7 13.4	— 5.2 3.7	184 20.6 14.7	ns
I_n to $\overline{Y}$	258	t_{PLH} t_{PHL}	1.5 3.3 5	— 2.9 2.1	91 10.2 7.3	— 2.8 2	100 11.2 8	ns
S to $\overline{Y}$	258	t_{PLH} t_{PHL}	1.5 3.3 5	— 4.8 3.5	153 17.1 12.2	— 4.7 3.4	168 18.8 13.4	ns
$\overline{OE}$ to $\overline{Y}$	258	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	1.5 3.3 5	— 5.3 3.8	167 18.7 13.4	— 5.2 3.7	184 20.6 14.7	ns
Power Dissipation Capacitance		C_{PD}§	—	130 Typ.		130 Typ.		pF
Input Capacitance		C_I	—	—	10	—	10	pF
3-State Output Capacitance		C_O	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				-40 to +85		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays: I_n to Y	257	t_{PLH} t_{PHL}	5†	2.8	9.7	2.7	10.7	ns
S to Y	257	t_{PLH} t_{PHL}	5	4	14	3.9	15.4	ns
$\overline{OE}$ to Y	257	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	4.1	14.6	4	16.1	ns
I_n to $\overline{Y}$	258	t_{PLH} t_{PHL}	5	2.4	8.5	2.3	9.3	ns
S to $\overline{Y}$	258	t_{PLH} t_{PHL}	5	4	14	3.9	15.4	ns
$\overline{OE}$ to $\overline{Y}$	258	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	4.1	14.6	4	16.1	ns
Power Dissipation Capacitance		C_{PD}§	—	130 Typ.		130 Typ.		pF
Input Capacitance		C_I	—	—	10	—	10	pF
3-State Output Capacitance		C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption per multiplexer.
For AC Series: $P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o)$
For ACT Series: $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$
where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC257, CD54/74AC258
CD54/74ACT257, CD54/74ACT258

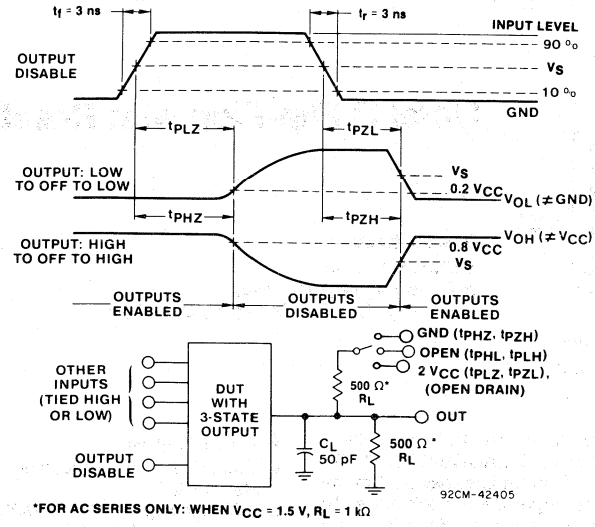

Fig. 1 - Three-state propagation delay waveforms and test circuit.

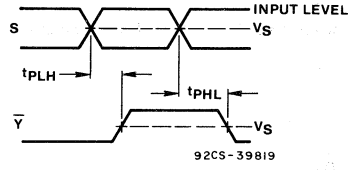

Fig. 2 - Select to output propagaton delays (AC/ACT258).

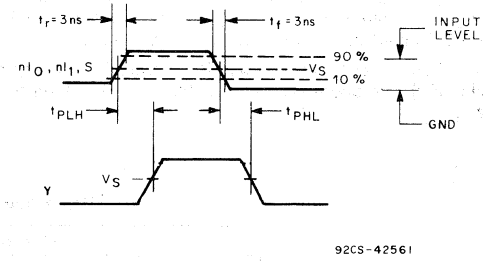

Fig. 3 - Inputs or select to output propagation delays (AC/ACT257).

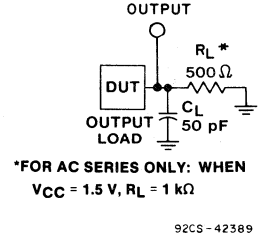

Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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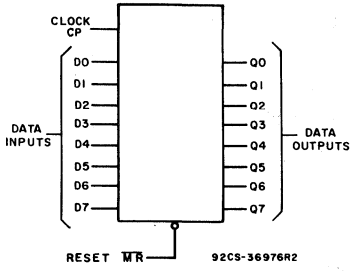
CD54/74AC273
CD54/74ACT273



FUNCTIONAL DIAGRAM

Octal D Flip-Flop with Reset

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 6.5 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF*

The RCA CD54/74AC273 and CD54/74ACT273 are octal D flip-flops with reset that use the RCA ADVANCED CMOS technology. Information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock.

The CD74AC273 and CD74ACT273 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC273 and CD54ACT273, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS
RESET ($\overline{MR}$)	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	⎍	H	H
H	⎍	L	L
H	L	X	Qo

H = High level (steady state)
L = Low level (steady state)
X = Irrelevant
⎍ = Transition from Low to High level
Qo = The level of Q before the indicated steady-state input conditions were established

File Number **1979**

CD54/74AC273
CD54/74ACT273

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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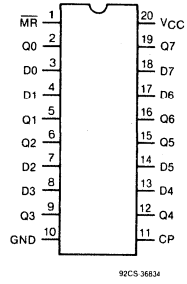

TERMINAL ASSIGNMENT

CD54/74AC273
CD54/74ACT273

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3.0	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3.0	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.40	—	1.40	—	1.40	—	V
		-0.05	3.0	2.90	—	2.90	—	2.90	—	
		-0.05	4.5	4.40	—	4.40	—	4.40	—	
		-4	3.0	2.58	—	2.48	—	2.40	—	
		-24	4.5	3.94	—	3.80	—	3.70	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3.0	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3.0	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI Icc	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.80	—	3.70	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.10	V
		24	4.5	—	0.36	—	0.44	—	0.50	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Dn	0.5
$\overline{MR}$	0.57
CP	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC273
CD54/74ACT273

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t_{SU}	1.5	2	—	2	—	ns
		3.3*	2	—	2	—	
		5†	2	—	2	—	
Hold Time	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Removal Time $\overline{MR}$ to CP	t_{REM}	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
$\overline{MR}$ Pulse Width	t_W	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
CP Pulse Width	t_W	1.5	55	—	63	—	ns
		3.3	6.1	—	7	—	
		5	4.4	—	5	—	
CP Frequency	f_{MAX}	1.5	9	—	8	—	MHz
		3.3	81	—	71	—	
		5	114	—	100	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t_{PLH}	1.5	—	154	—	169	ns
		3.3*	4.9	17.2	4.7	18.9	
	t_{PHL}	5†	3.5	12.3	3.4	13.5	
$\overline{MR}$ to Qn	t_{PLH}	1.5	—	154	—	169	ns
		3.3	4.9	17.2	4.7	18.9	
	t_{PHL}	5	3.5	12.3	3.4	13.5	
Power Dissipation Capacitance	C_{PD}§	—	45 Typ.		45 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V
†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per device.
$P_D = C_{PD} V_{CC}^2 f_i = \Sigma(C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC273
CD54/74ACT273

PREREQUISITE FOR SWITCHING — ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Data to CP Setup Time	t_{SU}	5*	2	—	2	—	ns
Hold Time	t_H	5	2	—	2	—	ns
Removal Time $\overline{MR}$ to CP	t_{REM}	5	2	—	2	—	ns
$\overline{MR}$ Pulse to Width	t_W	5	4.4	—	5	—	ns
CP Pulse Width	t_W	5	5.3	—	6	—	ns
CP Frequency	f_{max}	5	97	—	85	—	MHz

*min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn	t_{PLH} t_{PHL}	5*	3.5	12.3	3.4	13.5	ns
$\overline{MR}$ to Qn	t_{PLH} t_{PLH}	5	3.5	12.3	3.4	13.5	ns
Power Dissipation Capacitance	C_{PD}†	—	45 Typ.		45 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*min. is @ 5.5 V
max. is @ 4.5 V

†C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma(C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

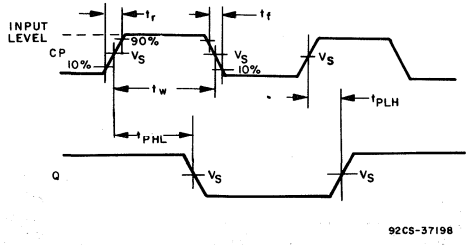

Fig. 1 - Propagation delay times and clock pulse width.

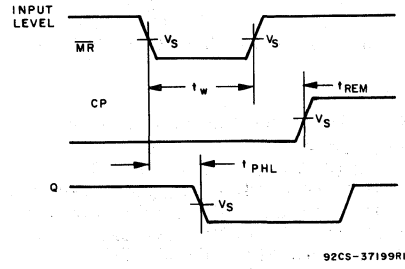

Fig. 2 - Prerequisite and propagation delay times for master reset

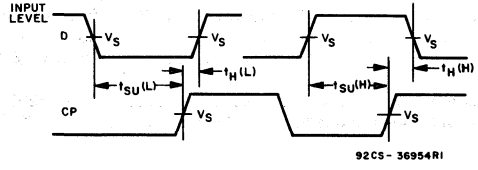

Fig. 3 - Prerequisite for clock.

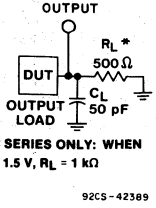

Fig. 4 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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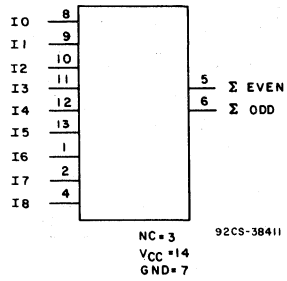
CD54/74AC280
CD54/74ACT280



FUNCTIONAL DIAGRAM

9-Bit Odd/Even Parity Generator/Checker

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 10 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC280 and CD54/74ACT280 9-bit odd/even parity generator/checkers use the RCA ADVANCED CMOS technology. Both even and odd parity outputs are available for checking or generating parity for words up to nine bits long. Even parity is indicated (ΣE output is HIGH) when an even number of data inputs is HIGH. Odd parity is indicated (ΣO output is HIGH) when an odd number of data inputs is HIGH. Parity checking for words larger than nine bits can be accomplished by tying the ΣE output to any input of an additional AC/ACT280 parity checker.

The CD74AC280 and CD74ACT280 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC280 and CD54ACT280, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

File Number **1957**

CD54/74AC280
CD54/74ACT280

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC280
CD54/74ACT280

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

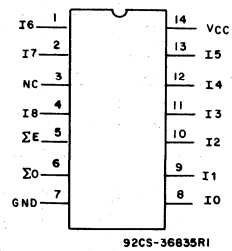
#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
All	1.43

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.



TERMINAL ASSIGNMENT

CD54/74AC280
CD54/74ACT280

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Input to ΣO	t_{PLH} t_{PHL}	1.5	—	239	—	263	ns
		3.3*	7.5	26	7.3	29	
		5†	5.4	19.1	5.3	21	
Any Input to ΣE	t_{PLH} t_{PHL}	1.5	—	227	—	250	ns
		3.3	7.2	25	7	28	
		5	5.2	18.2	5	20	
Power Dissipation Capacitance	C_{PD}§	—	115 Typ.		115 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

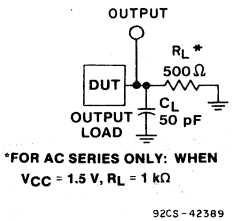
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

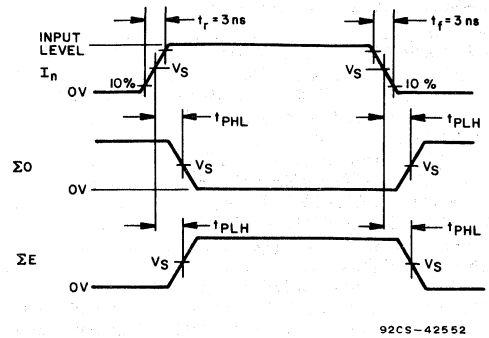
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Any Input to ΣO	t_{PLH} t_{PHL}	5†	5.6	19.6	5.4	21.6	ns
Any Input to ΣE	t_{PLH} t_{PHL}	5	5.6	19.6	5.4	21.6	ns
Power Dissipation Capacitance	C_{PD}§	—	115 Typ.		115 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.





	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 1 - Propagation delay times and test circuit.

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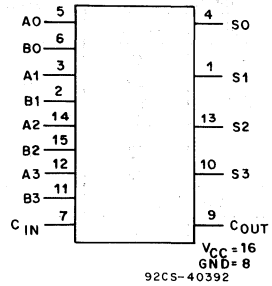
CD54/74AC283
CD54/74ACT283

Advance Information



FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

4-Bit Binary Full Adder with Fast Carry

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 8.2 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF*

The RCA-CD54/74AC283 and CD54/74ACT283 4-bit binary adders with fast carry use the RCA ADVANCED CMOS technology. These devices add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). When using positive logic, the carry-in input must be tied LOW if there is no carry-in.

The CD74AC283 and CD74ACT283 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC283 and CD54ACT283, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

File Number **1912**

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC283
CD54/74ACT283

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5		2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
A1, B1, A3, B3	1.33
A2, B2	1.5
A4, B4	1
C_{IN}	0.83

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A_n or B_n to C_{out}	t_{PLH}	1.5	—	199	—	219	ns
C_{in} to S_n	t_{PHL}	3.3*	6.3	22.4	6.2	24.6	
C_{in} to C_{out}		5†	4.5	16	4.4	17.6	
A_n or B_n to S_n	t_{PLH}	1.5	—	207	—	228	ns
	t_{PHL}	3.3	6.6	23.2	6.4	25.5	
		5	4.7	16.5	4.6	18.2	
Power Dissipation Capacitance	C_{PD}§	—	120 Typ.		120 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A_n or B_n to C_{out}	t_{PLH}	5†	4.5	16	4.4	17.6	ns
C_{in} to S_n	t_{PHL}						
C_{in} to C_{out}							
A_n or B_n to S_n	t_{PLH}	5	4.7	16.5	4.6	18.2	ns
	t_{PHL}						
Power Dissipation Capacitance	C_{PD}§	—	120 Typ.		120 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per function.
For AC Series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT Series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

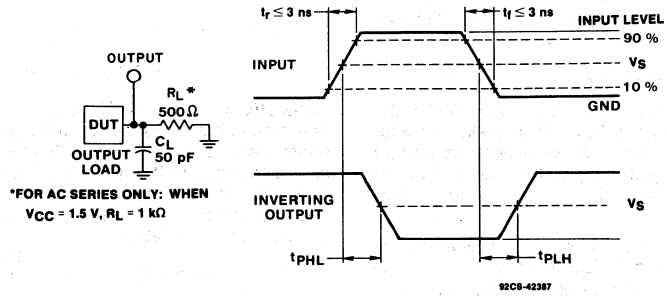
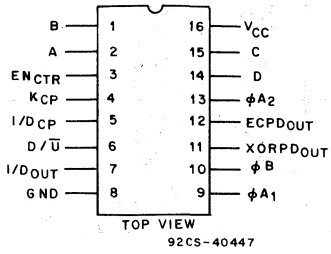


Fig. 1 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

CD54/74AC297
CD54/74ACT297

Product Preview



TERMINAL ASSIGNMENT

Digital Phase-Locked Loop

Type Features:

- *Digital design avoids analog compensation errors*
- *Easily cascadable for higher order loops*
- *Useful frequency range:*
  DC to 110 MHz typical (K-clock)
  DC to 70 MHz typical (I/D-clock)
- *Dynamically variable bandwidth*
- *Very narrow bandwidth attainable*
- *Power-on reset*
- *Output capability:*
  Standard - $XORPD_{OUT}$, $ECPD_{OUT}$
  Bus driver - I/D_{OUT}

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*

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The RCA-CD54/74AC297 and CD54/74ACT297 digital phase-locked loops use the RCA ADVANCED CMOS technology. They are high-speed silicon-gate CMOS devices that are pin-compatible with low-power Schottky TTL (LSTTL).

These devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. They contain all the necessary circuits, with the exception of the divide-by-N counter, to build first-order phase-locked loops.

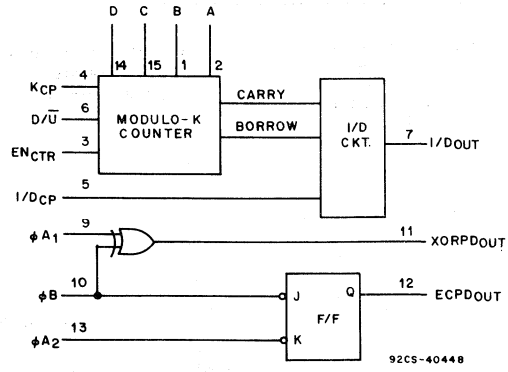
Both EXCLUSIVE-OR (XORPD) and edge-controlled phase detectors (ECPD) are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock range.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 2) or to cascade to higher order phase-locked loops.

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A to D inputs can maximize the overall performance of the digital phase-locked loop.

The CD54/74AC/ACT297 can perform the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked loop (DPLL) is not affected by VCC and temperature variations but depends solely on accuracies of the K-clock and loop propagation delays.

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be



FUNCTIONAL DIAGRAM

either HIGH or LOW all of the time depending on the direction of the phase error (ϕIN - ϕOUT). Within these limits the phase detector output varies linearly with the input phase error according to the gain K_d, which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between $\pm$ 1 according to the relation:

$$\text{phase detector output} = \frac{\%\ \text{HIGH} - \%\ \text{LOW}}{100}$$

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CD54/74AC297
CD54/74ACT297

The output of the phase detector will be $K_d\phi_e$, where the phase error

$$\phi_e = \phi_{IN} - \phi_{OUT}.$$

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain (K_d) for an XORPD is 4 because its output remains HIGH ($XORPD_{OUT}$ = 1) for a phase error of ¼ cycle.

Similarly, K_d for the ECPD is 2 since its output remains HIGH for a phase error of ½ cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a ϕ_e defined to be zero. For the basic DPLL system of Fig. 3, ϕ_e = 0 when the phase detector output is a square wave.

The XORPD inputs are ¼ cycle out of phase for zero phase error. For the ECPD, ϕ_e = 0 when the inputs are ½ cycle out of phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency Mf_c which is a multiple M of the loop center frequency f_c. When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(K_d\phi_eMf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is ½ of the input clock (I/D_{CP}). The input clock is just a multiple, 2N, of the loop center frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D_{OUT}. Thus the output of the I/D circuit will be $Nf_c + (K_d\phi_eMf_c)/2K$.

The output of the N-counter (or the output of the phase-locked loop) is thus:

$$f_o = f_c + (K_d\phi_eMf_c)/2KN.$$

If this result is compared to the equation for a first-order analog phase-locked loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for M = 2N.

Thus, the simple first-order phase-locked loop with an adjustable K-counter is the equivalent of an analog phase-locked loop with a programmable VCO gain.

The CD74AC297 and CD74ACT297 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC297 and CD54ACT297, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

K COUNTER FUNCTION TABLE
(DIGITAL CONTROL)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

FUNCTION TABLE
EXCLUSIVE-OR PHASE DETECTOR

ϕA_1	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

FUNCTION TABLE
EDGE-CONTROLLED PHASE DETECTOR

ϕA_2	ϕB	ECPD OUT
H or L	⎍	H
⎍	H or L	L
H or L	⎎	No Change
⎎	H or L	No Change

H = steady-state high level
L = steady-state low level
⎍ = transition from high to low
⎎ = transition from low to high

CD54/74AC297
CD54/74ACT297

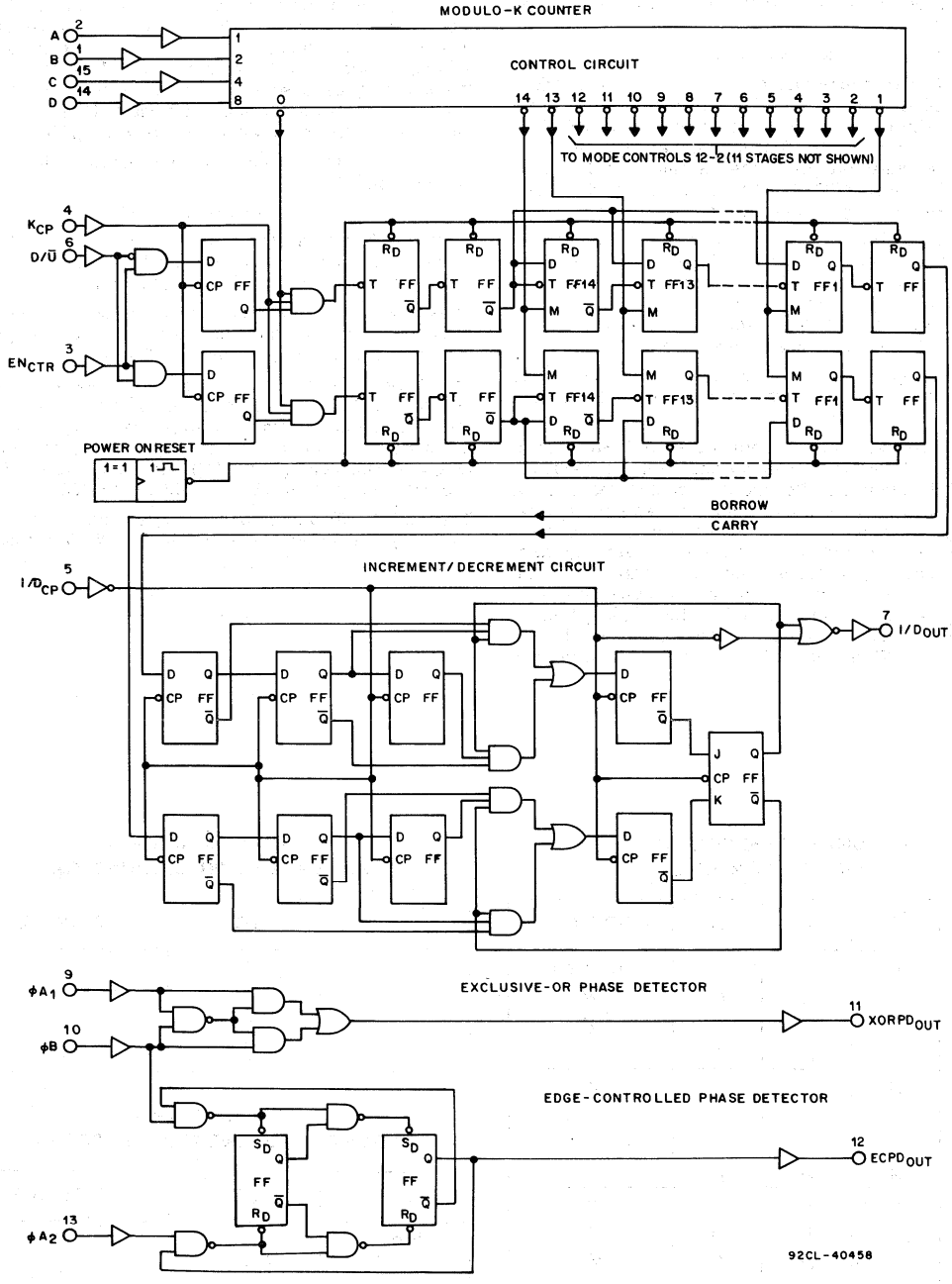


Fig. 1 - Logic diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

9

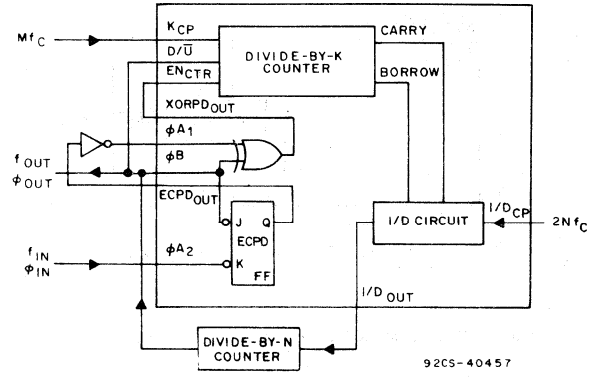


Fig. 2 - DPLL using both phase detectors in a ripple-cancellation scheme.

CD54/74AC297
CD54/74ACT297

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage V_{IL}			1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-8	4.5	3.94	—	3.8	—	3.7	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		8	4.5	—	0.36	—	0.44	—	0.5	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

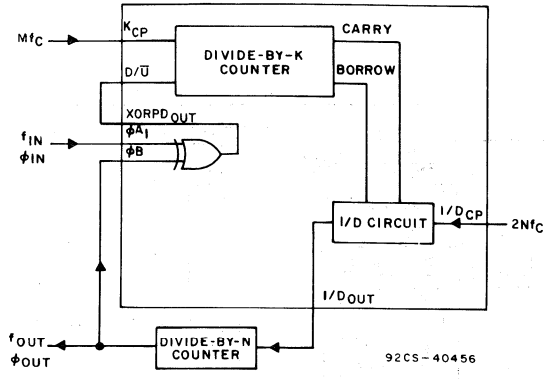


Fig. 3 - DPLL using EXCLUSIVE-OR phase detection.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-8	4.5	3.94	—	3.8	—	3.7	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		8	4.5	—	0.36	—	0.44	—	0.5	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
EN_{CTR}, $D/\overline{U}$	0.1
A, B, C, D, K_{CP}, ϕA_2	0.2
I/D_{CP}, ϕA_1, ϕB	0.5

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

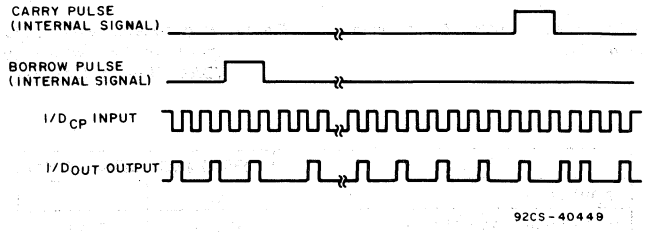


Fig. 4 - Timing diagram: I/D_{OUT} in-lock condition.

CD54/74AC297
CD54/74ACT297

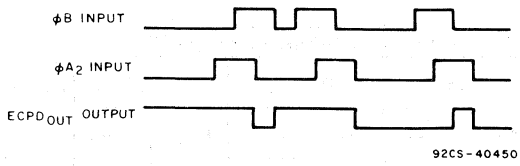


Fig. 5 - Timing diagram: edge-controlled phase comparator waveforms.

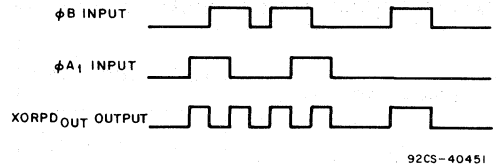


Fig. 6 - Timing diagram: EXCLUSIVE-OR phase detector waveforms.

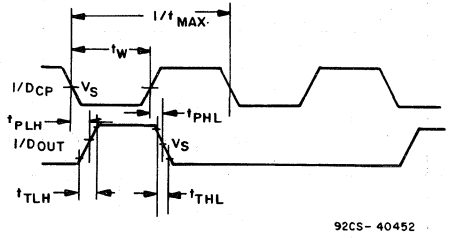


Fig. 7 - Waveforms showing the clock (I/D_{CP}) to output (I/D_{OUT}) propagation delays, clock pulse width, and maximum clock pulse frequency.

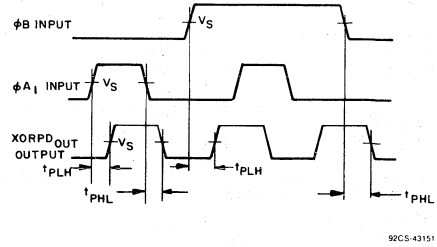


Fig. 8 - Waveforms showing the phase input (ϕB, ϕA_1) to output ($XORPD_{OUT}$) propagation delays.

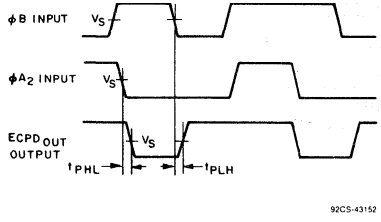
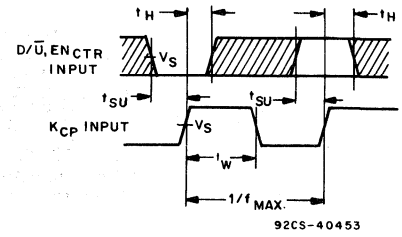


Fig. 9 - Waveforms showing the phase input (ϕB, ϕA_2) to output ($ECPD_{OUT}$) propagation delays.



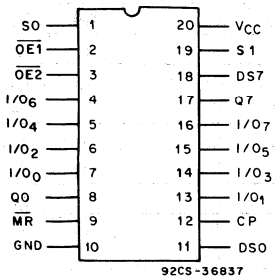
NOTE: THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE.

Fig. 10 - Waveforms showing the clock (K_{CP}) pulse width and maximum clock pulse frequency, and the input ($D/\overline{U}$, EN_{CTR}) to clock (K_{CP}) set-up and hold times.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Advance Information

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323



TERMINAL ASSIGNMENT

8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

CD54/74AC/ACT299 - Asynchronous Reset
CD54/74AC/ACT323 - Synchronous Reset

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  6 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

The RCA CD54/74AC299 and CD54/74AC323 and the CD54/74ACT299 and CD54/74ACT323 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices use the RCA ADVANCED CMOS technology. These registers have four synchronous-operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DSO, DS7), and the Parallel Data (I/O_0 - I/O_7) respond only to the LOW-TO-HIGH transition of the clock (CP) pulse. S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

With the CD54/74AC/ACT299, the Master Reset ($\overline{MR}$) is an asynchronous active-LOW input. When $\overline{MR}$ is LOW, the register is cleared regardless of the status of all other inputs. With the CD54/74AC/ACT323, the Master Reset ($\overline{MR}$) clears the register in sync with the clock input. The register can be expanded by cascading same units by tying the serial output (QO) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DSO) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DSO of the first stage.

The 3-state input/output (I/O) port has three modes of operation:

1. Both Output Enable ($\overline{OE1}$ and $\overline{OE2}$) inputs are LOW and S0 or S1 or both are LOW; the data in the register is present at the eight outputs.
2. When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a 3-state output and a CMOS buffer input.

The CD74AC/ACT299 and CD74AC/ACT323 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT299 and CD54AC/ACT323, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

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File Number **1958**

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

MODE SELECT — FUNCTION TABLE
REGISTER OPERATING MODES

FUNCTION	INPUTS							REGISTER OUTPUTS				
	$\overline{MR}$	CP	S0	S1	DS0	DS7	I/O_n	Q0	Q1	...	Q6	Q7
Reset (Clear)	L	X*	X	X	X	X	X	L	L	...	L	L
Shift Right	H	⎍	h	l	l	X	X	L	q_0	...	q_5	q_6
	H	⎍	h	l	h	X	X	H	q_0	...	q_5	q_6
Shift Left	H	⎍	l	h	X	l	X	q_1	q_2	...	q_7	L
	H	⎍	l	h	X	h	X	q_1	q_2	...	q_7	H
Hold (do nothing)	H	⎍	l	l	X	X	X	q_0	q_1	...	q_6	q_7
Parallel Load	H	⎍	h	h	X	X	l	L	L	...	L	L
	H	⎍	h	h	X	X	h	H	H	...	H	H

*On CD54/74AC/ACT323, CP must be in transition from the LOW-to-HIGH state to Reset (Clear).

MODE SELECT — FUNCTION TABLE
3-STATE I/O PORT OPERATING MODE

FUNCTION	INPUTS					INPUTS/OUTPUTS
	$\overline{OE1}$	$\overline{OE2}$	S0	S1	Qn (Register)	$I/O_0 \ldots I/O_7$
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	$Qn = I/O_n$	I/O_n = Inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

H = Input voltage high level.
h = Input voltage high one set-up time prior clock transition.
L = Input voltage low level.
l = Input voltage low one set-up time prior clock transition.
q_n = Lower case letters indicate the state of the referenced output one set-up time prior clock transition.
X = Voltage level on logic status don't care.
Z = Output in high-impedance state.
⎍ = Low-to-high clock transition.

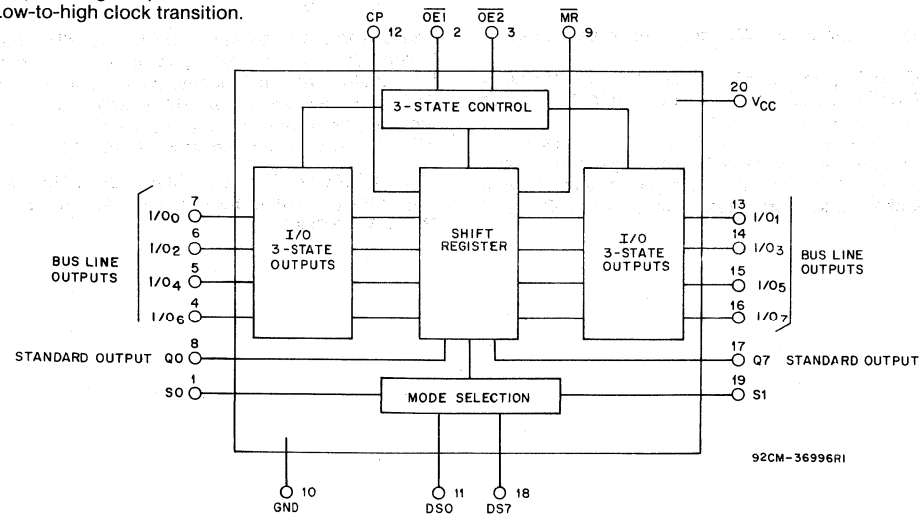

Fig. 1 - Functional diagram.

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
(For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-Stage Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*	
	299	323
S1, S0, $\overline{OE1}$, $\overline{OE2}$	0.83	0.83
I/O_0 - I/O_7, CP, DS0, DS7	0.67	0.67
$\overline{MR}$	1.33	0.67

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Setup Time S1, S0, to CP	t_{SU}	1.5 3.3* 5†	99 11.1 7.9	— — —	113 12.6 9	— — —	ns
Hold Time S1, S0 to CP	t_H	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns
Setup Time (I/O)n, DS0, DS7 to CP	t_{SU}	1.5 3.3 5	49 5.5 3.9	— — —	56 6.3 4.5	— — —	ns
Hold Time (I/O)n, DS0, DS7 to CP	t_{SU}	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns
Setup Time $\overline{MR}$ to CP (323)	t_{SU}	1.5 3.3 5	61 6.8 4.8	— — —	69 7.8 5.5	— — —	ns
Hold Time $\overline{MR}$ to CP (323)	t_H	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns
Maximum CP Frequency	f_{MAX}	1.5 3.3 5	9 78 108	— — —	8 68 95	— — —	MHz
CP Pulse Width	t_W	1.5 3.3 5	57 6.4 4.6	— — —	65 7.3 5.2	— — —	ns
$\overline{MR}$ Pulse Width	t_W	1.5 3.3 5	55 6.1 4.4	— — —	63 7 5	— — —	ns
Recovery Time $\overline{MR}$ to CP 299	t_{REC}	1.5 3.3 5	55 6.1 4.4	— — —	63 7 5	— — —	ns

*3.3 V: min. is @ 3 V
†5 V: min is @ 4.5 V

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t_{PLH}	1.5	—	147	—	162	ns
	t_{PHL}	3.3*	4.7	16.5	4.5	18.1	
		5†	3.3	11.7	3.2	12.9	
CP to (I/O)n	t_{PLH}	1.5	—	154	—	169	ns
	t_{PHL}	3.3	4.9	17.2	4.7	18.9	
		5	3.5	12.3	3.4	13.5	
$\overline{MR}$ to Q0, Q7 (299 only)	t_{PLH}	1.5	—	127	—	140	ns
	t_{PHL}	3.3	4	14.3	3.9	15.7	
		5	2.9	10.2	2.8	11.2	
$\overline{MR}$ to (I/O)n	t_{PLH}	1.5	—	158	—	174	ns
	t_{PHL}	3.3	5	17.7	4.9	19.5	
		5	3.6	12.6	3.5	13.9	
Enable and Disable Times	t_{PZL}	1.5	—	169	—	186	ns
	t_{PZH}	3.3	5.8	20.4	5.6	22.4	
	t_{PLZ}	5	3.8	13.5	3.7	14.9	
	t_{PHZ}						
Power Dissipation Capacitance	C_{PD}§	—	280 Typ.		280 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per function.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Setup Time S1, S0 to CP	t_{SU}	5*	7.9	—	9	—	ns
Hold Time S1, S0 to CP	t_H	5	0	—	0	—	ns
Setup Time (I/O)n, DS0, DS7 to CP	t_{SU}	5	3.9	—	4.5	—	ns
Hold Time (I/O)n, DS0, DS7 to CP	t_H	5	0	—	0	—	ns
Setup Time $\overline{MR}$ to CP (323)	t_{SU}	5*	4.8	—	5.5	—	ns
Hold Time $\overline{MR}$ to CP (323)	t_H	5	0	—	0	—	ns
Maximum CP Frequency	f_{max}	5	103	—	90	—	MHz
CP Pulse Width	t_W	5	4.8	—	5.5	—	ns
$\overline{MR}$ Pulse Width	t_W	5	4.4	—	5	—	ns
Recovery Time $\overline{MR}$ to CP (299)	t_{REC}	5	4.4	—	5	—	ns

*5 V: min. is @ 4.5 V

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CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Q0, Q7	t_{PLH} t_{PHL}	5*	3.3	11.7	3.2	12.9	ns
CP to (I/O)n	t_{PLH} t_{PHL}	5	3.7	13.2	3.6	14.5	ns
$\overline{MR}$ to Q0, Q7 (299 only)	t_{PLH} t_{PHL}	5	3.1	11.1	3.1	12.2	ns
$\overline{MR}$ to (I/O)n	t_{PLH} t_{PHL}	5	4.8	16.9	4.7	18.6	ns
Enable and Disable Times	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.8	13.5	3.7	14.9	ns
Power Dissipation Capacitance	C_{PD}§	—	280 Typ.		280 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per function.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

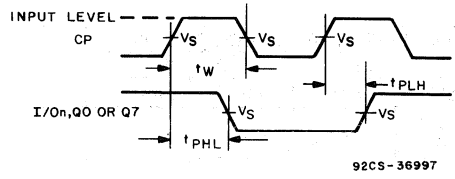


Fig. 2 - Clock prerequisite and propagation delays.

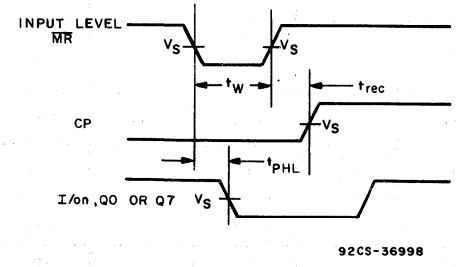
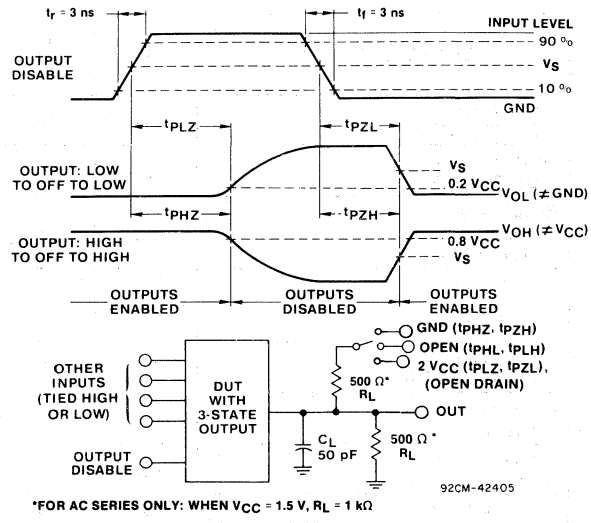


Fig. 3 - Master Reset prerequisite and propagation delays.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 4 - Three-state propagation delay times and test circuit.

CD54/74AC299, CD54/74AC323
CD54/74ACT299, CD54/74ACT323

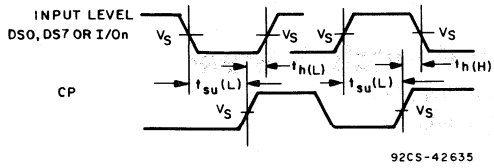


Fig. 5 - Data prerequisite times.

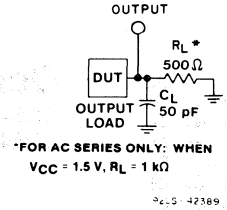


Fig. 6 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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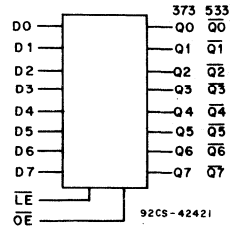
CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533

Advance Information



FUNCTIONAL DIAGRAM

Octal Transparent Latch, 3-State

CD54/74AC/ACT373 - Non-Inverting
CD54/74AC/ACT533 - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  4.3 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA-CD54/74AC373 and CD54/74AC533 and the CD54/74ACT373 and CD54/74ACT533 octal transparent 3-state latches use the RCA ADVANCED CMOS technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD74AC/ACT373 and CD74AC/ACT533 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT373 and CD54AC/ACT533, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - Fanout to 15 FAST ICs*
  - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

$\overline{\text{Output Enable}}$	$\overline{\text{Latch Enable}}$	Data	AC/ACT373 Output	AC/ACT533 Output
L	H	H	H	L
L	H	L	L	H
L	L	I	L	H
L	L	h	H	L
H	X	X	Z	Z

Note:
L = Low voltage level
H = High voltage level
I = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition.
X = Don't Care
Z = High Impedance State

File Number **1882**

CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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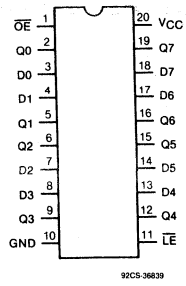
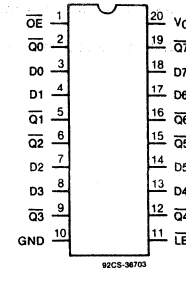
TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC373, CD54/74ACT373



CD54/74AC533, CD54/74ACT533

CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	ACT373	ACT533
$\overline{OE}$	0.87	0.87
Dn	0.5	0.5
$\overline{LE}$	0.8	0.8

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
$\overline{LE}$ Pulse Width	t_W	1.5	44	—	50	—	ns
		3.3*	4.9	—	5.6	—	
		5†	3.5	—	4	—	
Setup Time Data to $\overline{LE}$	t_{SU}	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Hold Time Data to $\overline{LE}$	t_H	1.5	33	—	38	—	ns
		3.3	3.7	—	4.2	—	
		5	2.6	—	3	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn 373	t_{PLH} t_{PHL}	1.5	—	96	—	106	ns
		3.3*	3.1	10.8	3	11.9	
		5†	2.2	7.7	2.1	8.5	
533	t_{PLH} t_{PHL}	1.5	—	119	—	131	ns
		3.3	3.8	13.4	3.7	14.7	
		5	2.7	9.5	2.6	10.5	
$\overline{LE}$ on Qn 373	t_{PLH} t_{PHL}	1.5	—	136	—	150	ns
		3.3	4.3	15.2	4.2	16.8	
		5	3.1	10.9	3	12	
533	t_{PLH} t_{PHL}	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
Output Enable Times	t_{PZL} t_{PZH}	1.5	—	119	—	131	ns
		3.3	4.1	14.4	4	15.8	
		5	2.7	9.5	2.6	10.5	
Output Disable Times	t_{PLZ} t_{PHZ}	1.5	—	131	—	144	ns
		3.3	3.7	13.1	3.6	14.4	
		5	3	10.5	2.9	11.5	
Power Dissipation Capacitance	C_{PD}§	—	63 Typ.		63 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per latch.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
$\overline{LE}$ Pulse Width	t_W	5†	3.6	—	4	—	ns
Setup Time Data to $\overline{LE}$	t_{SU}	5	2	—	2	—	ns
Hold Time Data to $\overline{LE}$	t_H	5	2.7	—	3	—	ns

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn							
373	t_{PLH}	5†	2.7	9.5	2.6	10.4	ns
533	t_{PHL}		3	10.4	2.9	11.4	
$\overline{LE}$ to Qn							
373	t_{PLH}	5	3.1	11.4	3	12.5	ns
533	t_{PHL}						
Output Enable Times	t_{PZL} t_{PZH}	5	3.5	12.3	3.4	13.5	ns
Output Disable Times	t_{PLZ} t_{PHZ}	5	3.2	11.4	3.1	12.5	ns
Power Dissipation Capacitance	C_{PD}§	—	63 Typ.		63 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per latch.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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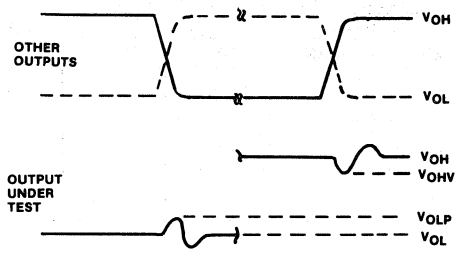
CD54/74AC373, CD54/74AC533
CD54/74ACT373, CD54/74ACT533

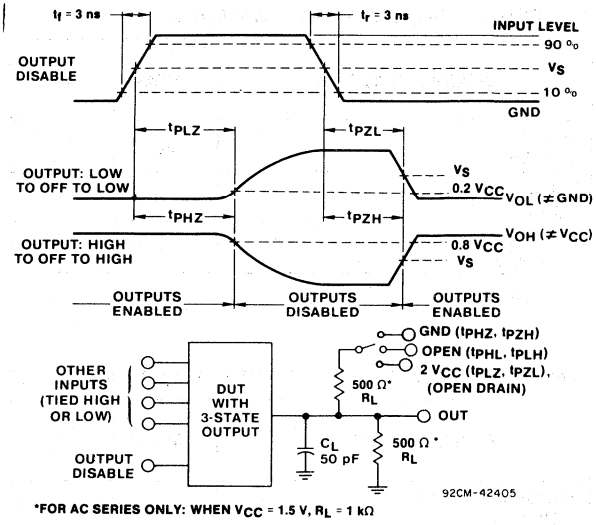
PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 2 - Three-state propagation delay waveforms and test circuit.

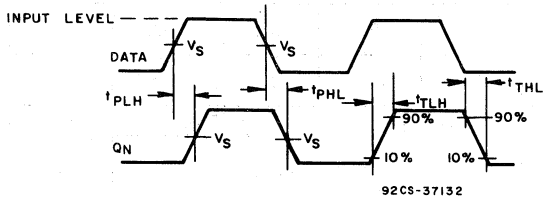


Fig. 3 - Data to Qn output propagation delays and output transistion times.

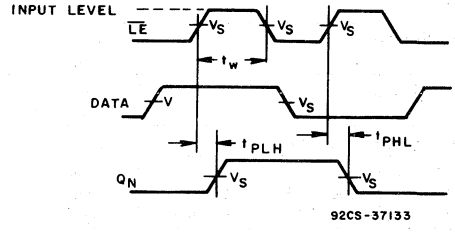


Fig. 4 - Latch enable propagation delays.

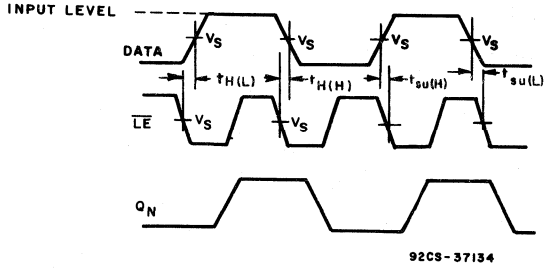
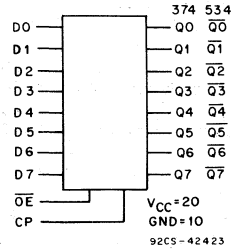


Fig. 5 - Latch enable prerequisite times.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Advance Information

CD54/74AC374, CD54/74AC534
CD54/74ACT374, CD54/74ACT534



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flops, 3-State
Positive-Edge Triggered
CD54/74AC/ACT374 - Non-Inverting
CD54/74AC/ACT534 - Inverting

Type Features:
- *Buffered inputs*
- *Typical propagation delay:*
  5 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA-CD54/74AC374 and CD54/74AC534 and the CD54/74ACT374 and CD54/74ACT534 octal D-type, 3-state, positive-edge triggered flip-flops use the RCA ADVANCED CMOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The CD54/74AC/ACT374 and CD54/74AC/ACT534 share the same pin configurations, but the CD54/74AC/ACT374 outputs are non-inverted while the CD54/74AC/ACT534 devices have inverted outputs. (For flow-through pin configurations, see CD54/74AC/ACT564 and CD54/74AC/ACT574.)

The CD74AC/ACT374 and CD74AC/ACT534 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT374 and CD54AC/ACT534, available in chip form (H suffix), are operable over the -55 to +125×C temperature range.

Family Features:
- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

**FAST is a Registered Trademark of Fairchild Semiconductor Corp.*

TRUTH TABLE

INPUTS			OUTPUTS	
			374	534
$\overline{OE}$	CP	Dn	Qn	Qn
L	⎍⎾	H	H	L
L	⎍⎾	L	L	H
L	L	X	QO	QO
H	X	X	Z	Z

H = High level (steady state)
L = Low level (steady state)
X = Don't care
⎍⎾ = Transition from low to high level
QO = The level of Q before the indicated steady-state input conditions were established
Z = High impedance

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File Number **1883**

CD54/74AC374, CD54/74AC534
CD54/74ACT374, CD54/74ACT534

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

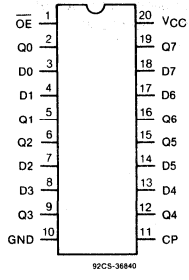
*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

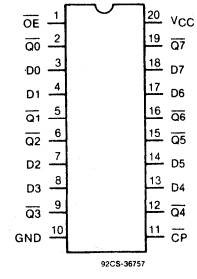
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT374



CD54/74AC/ACT534

CD54/74AC374, CD54/74AC534
CD54/74ACT374, CD54/74ACT534

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC374, CD54/74AC534
CD54/74ACT374, CD54/74ACT534

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
D, $\overline{OE}$	0.7
CP	1.17

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC374, CD54/74AC534
CD54/74ACT374, CD54/74ACT534

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t_W	1.5	44	—	50	—	ns
		3.3*	4.9	—	5.6	—	
		5†	3.5	—	4	—	
Setup Time Data to Clock	t_{SU}	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Hold Time Data to Clock	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Maximum Clock Frequency	f_{MAX}	1.5	11	—	10	—	MHz
		3.3	101	—	89	—	
		5	143	—	125	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q AC374	t_{PLH} t_{PHL}	1.5	—	123	—	135	ns
		3.3*	3.9	13.7	3.8	15.1	
		5†	2.8	9.8	2.7	10.8	
Clock to $\overline{Q}$ AC534	t_{PLH} t_{PHL}	1.5	—	128	—	141	ns
		3.3	4.1	14.4	4	15.8	
		5	2.9	10.3	2.8	11.3	
Output Enable to Q, $\overline{Q}$	t_{PZL} t_{PZH}	1.5	—	165	—	181	ns
		3.3	5.6	19.8	5.5	21.8	
		5	3.7	13.2	3.6	14.5	
Output Disable to Q, $\overline{Q}$	t_{PLZ} t_{PHZ}	1.5	—	165	—	181	ns
		3.3	4.7	16.5	4.5	18.1	
		5	3.7	13.2	3.6	14.5	
Power Dissipation Capacitance	C_{PD}§	—	67 Typ.		67 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_O C_L$ where f_i = input frequency
f_O = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC374, CD54/74AC534
CD54/74ACT374, CD54/74ACT534

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t_W	5†	3.9	—	4.5	—	ns
Setup Time Data to Clock	t_{SU}	5	2	—	2	—	ns
Hold Time Data to Clock	t_H	5	2.6	—	3	—	ns
Maximum Clock Frequency	f_{MAX}	5	125	—	110	—	MHz

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

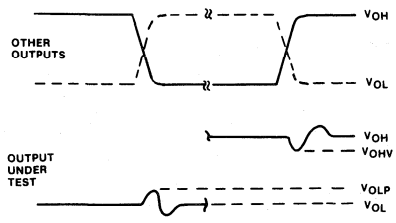
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q ACT374	t_{PLH} t_{PHL}	5†	2.9	10.2	2.8	11.2	ns
Clock to $\overline{Q}$ ACT534	t_{PLH} t_{PHL}	5	3	10.6	2.9	11.7	ns
Output Enable and Disable to Q ACT374	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.7	13.2	3.6	14.5	ns
Output Enable and Disable to $\overline{Q}$ ACT534	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.7	13.2	3.6	14.5	ns
Power Dissipation Capacitance	C_{PD}§	—	67 Typ.		67 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip flop.
$P_D = C_{PD} V_{CC}^2 f_i + V_{CC}^2 f_o C_L + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC374, CD54/74AC534
CD54/74ACT374, CD54/74ACT534

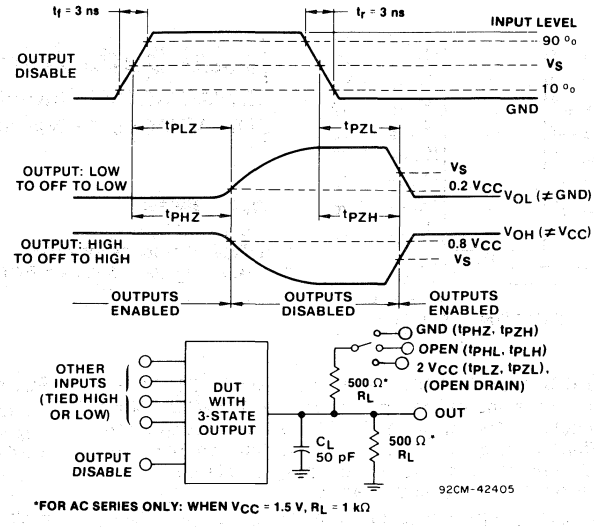
PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

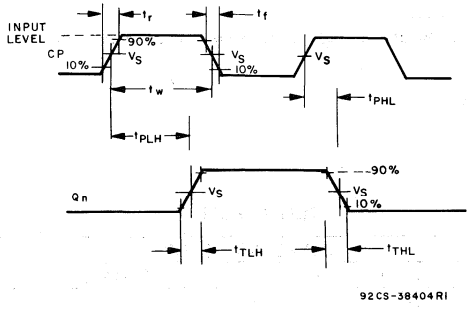
92CS-42406

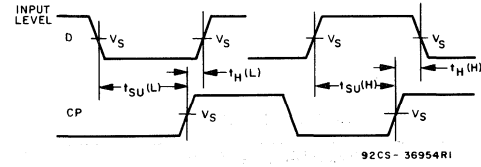
Fig. 1 - Simultaneous switching transient waveforms.



**For AC series only: When V_{CC} = 1.5V, R_L = 1 kΩ*

Fig. 2 - Three-state propagation delay waveforms and test circuit.





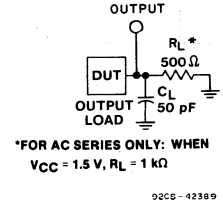


Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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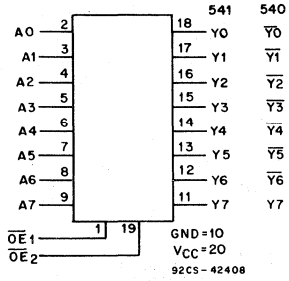
CD54/74AC540, CD54/74AC541
CD54/74ACT540, CD54/74ACT541



FUNCTIONAL DIAGRAM

Octal Buffer/Line Drivers, 3-State

CD74AC/ACT540 - Inverting
CD74AC/ACT541 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  4.5 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA-CD54/74AC540, -541 and CD54/74ACT540, -541 octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT540 are inverting 3-state buffers having two active-LOW output enables. The CD54/74AC/ACT541 are non-inverting 3-state buffers having two active-LOW ouput enables.

The CD74AC540, -541 and CD74ACT540, -541 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85° C); and Extended Industrial/Military (-55 to +125° C).

The CD54AC540, -541 and CD54ACT540, -541, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST®/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST® ICs*
  - *Drives 50-ohm transmission lines*

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

CD54/74AC/ACT540		
INPUTS		OUTPUTS
$\overline{OE1}$, $\overline{OE2}$	A	Y
L	L	H
L	H	L
H	X	Z

TRUTH TABLE

CD54/74AC/ACT541		
INPUTS		OUTPUTS
$\overline{OE1}$, $\overline{OE2}$	A	Y
L	L	H
L	H	L
H	X	Z

H = High Voltage
L = Low Voltage
X = Immaterial
Z = High Impedance

File Number **1857**

CD54/74AC540, CD54/74AC541
CD54/74ACT540, CD54/74ACT541

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

* For up to 4 outputs per device; add ± 25 mA for each additional output.

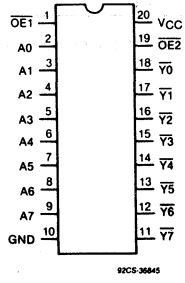
RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

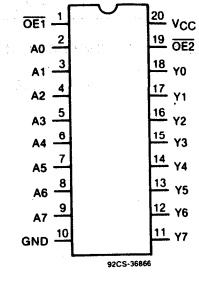
*Unless otherwise specified, all voltages are referenced to ground.

9

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT540



CD54/74AC/ACT541

CD54/74AC540, CD54/74AC541
CD54/74ACT540, CD54/74ACT541

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC540, CD54/74AC541
CD54/74ACT540, CD54/74ACT541

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
		#, *	-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
		#, *	75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	540	541
DATA	1.42	0.5
$\overline{OE1}$, $\overline{OE2}$	1.3	1.3

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC540, CD54/74AC541
CD54/74ACT540, CD54/74ACT541

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output AC540	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 2.4 1.8	77 8.6 6.2	— 2.4 1.7	85 9.5 6.8	ns
AC541	t_{PLH} t_{PHL}	1.5 3.3 5	— 2.8 2.1	89 9.9 7.1	— 2.7 2	98 10.9 7.8	ns
Enable, to Output to Output	t_{PZL} t_{PZH}	1.5 3.3 5	— 4.6 3.1	136 16.4 10.9	— 4.5 3	150 18 12	ns
Disable to Output to Output	t_{PLZ} t_{PHZ}	1.5 3.3 5	— 3.9 3.1	136 13.6 10.9	— 3.8 3	150 15 12	ns
Power Dissipation Capacitance AC540 AC541	C_{PD}‡	— —	60 Typ. 60 Typ.		60 Typ. 60 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to =125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output ACT540	t_{PLH} t_{PHL}	5†	1.9	6.5	1.8	7.2	ns
ACT541	t_{PLH} t_{PHL}	5†	2.1	7.5	2.1	8.2	ns
Enable to Output	t_{PZL} t_{PZH}	5	3.5	12.2	3.4	13.4	ns
Disable to Output	t_{PLZ} t_{PHZ}	5	3.5	12.2	3.4	13.4	
Power Dissipation Capacitance ACT540 ACT541	C_{PD}§	— —	60 Typ. 60 Typ.		60 Typ. 60 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

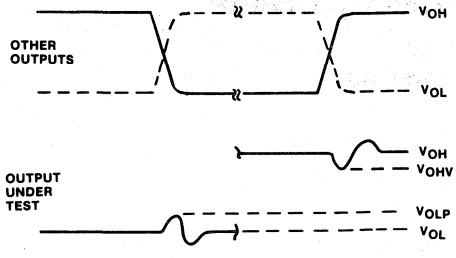
*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per channel.
For AC series, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

CD54/74AC540, CD54/74AC541
CD54/74ACT540, CD54/74ACT541

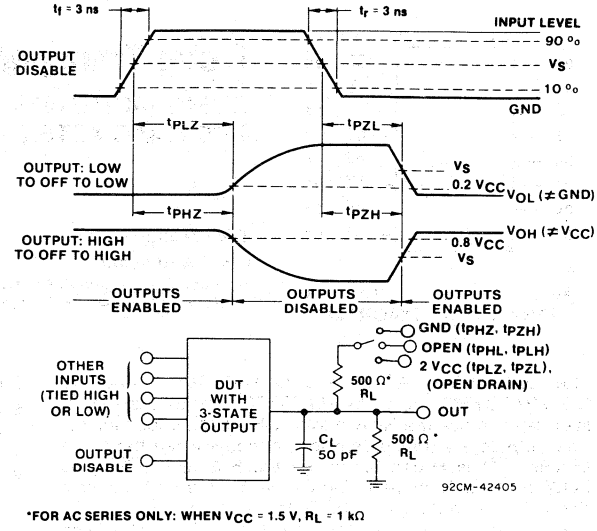
PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

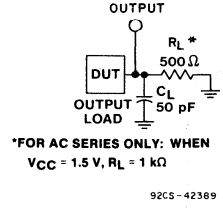
92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 2 - Three-state propagation delay waveforms and test circuit.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

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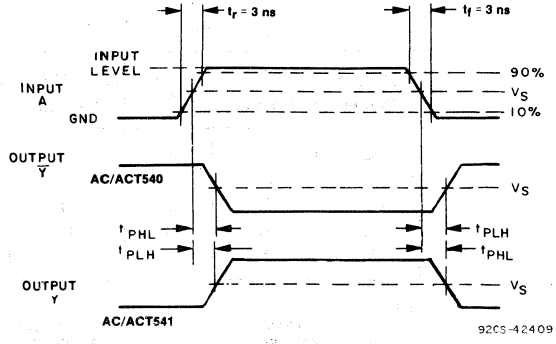

Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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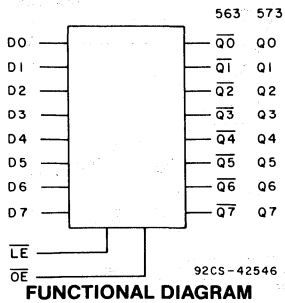
CD54/74AC563, CD54/74AC573
CD54/74ACT563, CD54/74ACT573



FUNCTIONAL DIAGRAM

Octal Transparent Latch, 3-State

CD54/74AC/ACT563 - Inverting
CD54/74AC/ACT573 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  4.3 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA-CD54/74AC563 and CD54/74AC573 and the CD54/74ACT563 and CD54/74ACT573 octal transparent 3-state latches use the RCA ADVANCED CMOS technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD74AC/ACT563 and CD74AC/ACT573 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70° C); Industrial (-40 to +85° C); and Extended Industrial/Military (-55 to +125° C).

The CD54AC/ACT563 and CD54AC/ACT573, available in chip form (H suffix), are operable over the -55 to +125° C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

$\overline{\text{Output}}$ Enable	$\overline{\text{Latch}}$ Enable	Data	AC/ACT563 Output	AC/ACT573 Output
L	H	H	L	H
L	H	L	H	L
L	L	l	H	L
L	L	h	L	H
H	X	X	Z	Z

Note:
L = Low voltage level
H = High voltage level
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition.
X = Don't Care
Z = High Impedance State

File Number **1956**

CD54/74AC563, CD54/74AC573
CD54/74ACT563, CD54/74ACT573

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
(For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V(AC Types)	0	50	ns/V
at 3.6 V to 5.5 V(AC Types)	0	20	ns/V
at 4.5 V to 5.5 V(ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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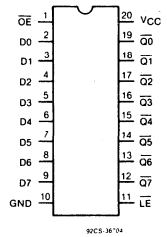
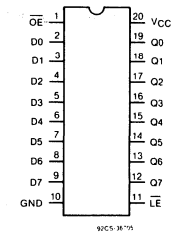
TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC563, CD54/74ACT563



CD54/74AC573, CD54/74ACT573

CD54/74AC563, CD54/74AC573
CD54/74ACT563, CD54/74ACT573

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}		-0.05	1.5	1.4	—	1.4	—	1.4	—	V
	V_{IH}	-0.05	3	2.9	—	2.9	—	2.9	—	
	or	-0.05	4.5	4.4	—	4.4	—	4.4	—	
	V_{IL}	-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}		0.05	1.5	—	0.1	—	0.1	—	0.1	V
	V_{IH}	0.05	3	—	0.1	—	0.1	—	0.1	
	or	0.05	4.5	—	0.1	—	0.1	—	0.1	
	V_{IL}	12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC563, CD54/74AC573
CD54/74ACT563, CD54/74ACT573

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	ACT563	ACT573
$\overline{OE}$	0.87	0.87
Dn	0.5	0.5
$\overline{LE}$	0.8	0.8

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC563, CD54/74AC573
CD54/74ACT563, CD54/74ACT573

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
$\overline{LE}$ Pulse Width	t_W	1.5	44	—	50	—	ns
		3.3*	4.9	—	5.6	—	
		5†	3.5	—	4	—	
Setup Time Data to $\overline{LE}$	t_{SU}	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Hold Time Data to $\overline{LE}$	t_H	1.5	33	—	38	—	ns
		3.3	3.7	—	4.2	—	
		5	2.6	—	3	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn AC563	t_{PLH} t_{PHL}	1.5	—	119	—	131	ns
		3.3*	3.8	13.4	3.7	14.7	
		5†	2.7	9.5	2.6	10.5	
AC573	t_{PLH} t_{PHL}	1.5	—	96	—	106	ns
		3.3	3.1	10.8	3	11.9	
		5	2.2	7.7	2.1	8.5	
$\overline{LE}$ on Qn AC563	t_{PLH} t_{PHL}	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
AC573	t_{PLH} t_{PHL}	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
Output Enable Times	t_{PZL} t_{PZH}	1.5	—	119	—	131	ns
		3.3	4.1	14.4	4	15.8	
		5	2.7	9.5	2.6	10.5	
Output Disable Times	t_{PLZ} t_{PHZ}	1.5	—	131	—	144	ns
		3.3	3.7	13.1	3.6	14.4	
		5	3	10.5	2.9	11.5	
Power Dissipation Capacitance	C_{PD}§	—	63 Typ.		63 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per latch.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC563, CD54/74AC573
CD54/74ACT563, CD54/74ACT573

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
$\overline{LE}$ Pulse Width	t_w	5†	3.5	—	4	—	ns
Setup Time Data to $\overline{LE}$	t_{SU}	5	2	—	2	—	ns
Hold Time Data to $\overline{LE}$	t_H	5	2.6	—	3	—	ns

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Qn	t_{PLH} t_{PHL}						
563		5†	2.9	10.4	2.9	11.4	ns
573			2.7	9.4	2.6	10.4	
$\overline{LE}$ to Qn 563 573	t_{PLH} t_{PHL}	5	3.2	11.4	3.1	12.5	ns
Output Enable Times	t_{PZL} t_{PZH}	5	3.5	12.3	3.4	13.5	ns
Output Disable Times	t_{PLZ} t_{PHZ}	5	3.2	11.4	3.1	12.5	ns
Power Dissipation Capacitance	C_{PD}§	—	63 Typ.		63 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per latch.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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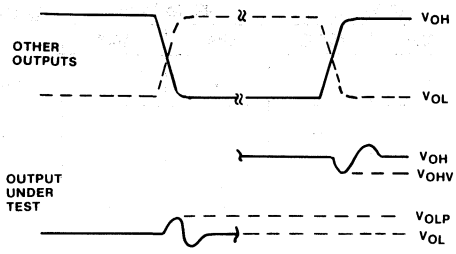
CD54/74AC563, CD54/74AC573
CD54/74ACT563, CD54/74ACT573

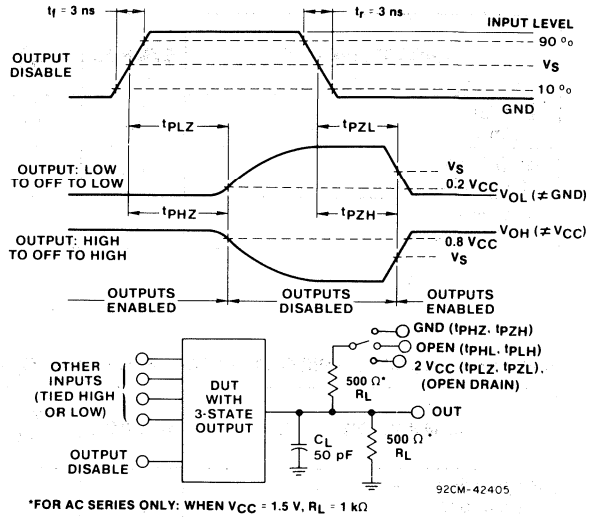
PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR = 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 2 - Three-state propagation delay waveforms and test circuit.

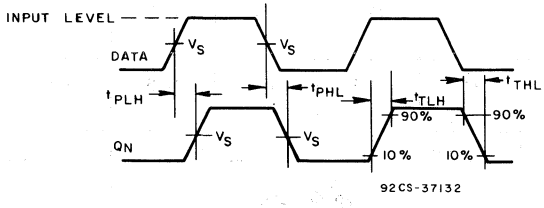


Fig. 3 - Data to Qn output propagation delays.

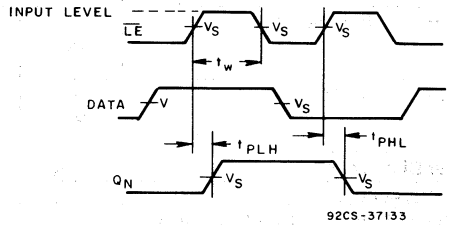


Fig. 4 - Latch enable propagation delays.

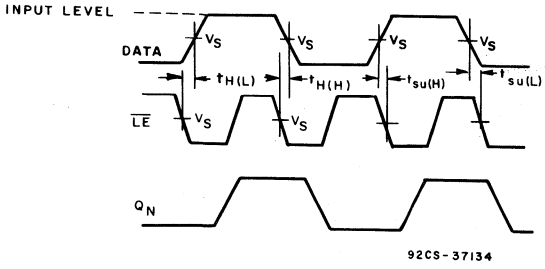


Fig. 5 - Latch enable prerequisite times.

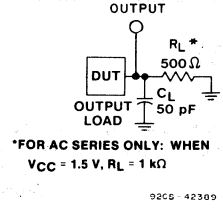
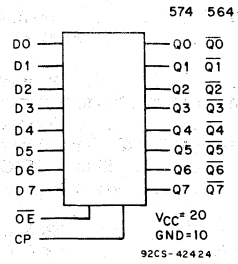


Fig. 6 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Advance Information

CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574



FUNCTIONAL DIAGRAM

Octal D-Type Flip-Flop, 3-State
Positive-Edge-Triggered

CD54/74AC/ACT564 - Inverting
CD54/74AC/ACT574 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  6.5 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA-CD54/74AC564 and CD54/74AC574 and the CD54/74ACT564 and CD54/74ACT574 octal D-type, 3-state, positive-edge-triggered flip-flops use the RCA ADVANCED CMOS technology. The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the 3-state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The CD54/74AC/ACT564 and CD54/74AC/ACT574 share the same pin configurations; the CD54/74AC/ACT564, however, has inverted outputs and the CD54/74AC/ACT574 has non-inverted outputs.

The CD74AC/ACT564 and CD74AC/ACT574 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70° C); Industrial (-40 to +85° C); and Extended Industrial/Military (-55 to +125° C).

The CD54AC/ACT564 and CD54AC/ACT574, available in chip form (H suffix), are operable over the -55 to +125° C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS			OUTPUTS	
			564	574
$\overline{OE}$	CP	Dn	$\overline{Qn}$	Qn
L	⎍	H	L	H
L	⎍	L	H	L
L	L	X	$\overline{QO}$	QO
H	X	X	Z	Z

H = High level (steady state)
L = Low level (steady state)
X = Don't care
⎍ = Transition from low to high level
QO = The level of Q before the indicated steady-state input conditions were established
$\overline{QO}$ = The level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Z = High impedance

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File Number **1948**

CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

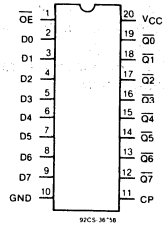
*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

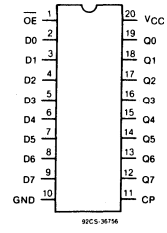
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT564



CD54/74AC/ACT574

CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL} #, *	0.05	4.5	—	±0.1	—	±.1	—	±.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOADS*
D, $\overline{OE}$	0.7
CP	1.17

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t_W	1.5	44	—	50	—	ns
		3.3*	4.9	—	5.6	—	
		5†	3.5	—	4	—	
Setup Time Data to Clock	t_{SU}	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Hold Time Data to Clock	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Maximum Clock Frequency	f_{MAX}	1.5	11	—	10	—	MHz
		3.3	101	—	89	—	
		5	143	—	125	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q AC574	t_{PLH} t_{PHL}	1.5	—	123	—	135	ns
		3.3*	4	13.7	3.8	15.1	
		5†	2.9	9.8	2.7	10.8	
Clock to $\overline{Q}$ AC564	t_{PLH} t_{PHL}	1.5	—	128	—	141	ns
		3.3	4.1	14.4	4	15.8	
		5	2.9	10.3	2.8	11.3	
Output Enable to Q, $\overline{Q}$	t_{PZL} t_{PZH}	1.5	—	165	—	181	ns
		3.3	5.6	19.2	5.5	21.8	
		5	3.7	13.2	3.6	14.5	
Output Disable to Q, $\overline{Q}$	t_{PLZ} t_{PHZ}	1.5	—	165	—	181	ns
		3.3	4.7	16.5	4.5	18.1	
		5	3.7	13.2	3.6	14.5	
Power Dissipation Capacitance	C_{PD}§	—	67 Typ.		67 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_O C_L$ where f_i = input frequency
f_O = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Clock Pulse Width	t_W	5†	3.9	—	4.5	—	ns
Setup Time Data to Clock	t_{SU}	5	2	—	2	—	ns
Hold Time Data to Clock	t_H	5	2.6	—	3	—	ns
Maximum Clock Frequency	f_{MAX}	5	125	—	110	—	MHz

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

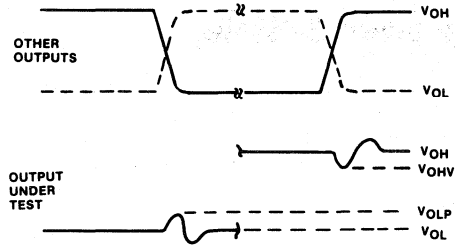
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) -°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Clock to Q ACT574	t_{PLH} t_{PHL}	5†	2.9	10.2	2.8	11.2	ns
Clock to $\overline{Q}$ ACT564	t_{PLH} t_{PHL}	5	3	10.6	2.9	11.7	ns
Output Enable and Disable to Q ACT574	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.7	13.2	3.6	14.5	ns
Output Enable and Disable to $\overline{Q}$ ACT564	t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	5	3.7	13.2	3.6	14.5	ns
Power Dissipation Capacitance	C_{PD}§	—	67 Typ.		67 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip flop.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma V_{CC}^2 f_O C_L + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_O = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC564, CD54/74AC574
CD54/74ACT564, CD54/74ACT574

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.

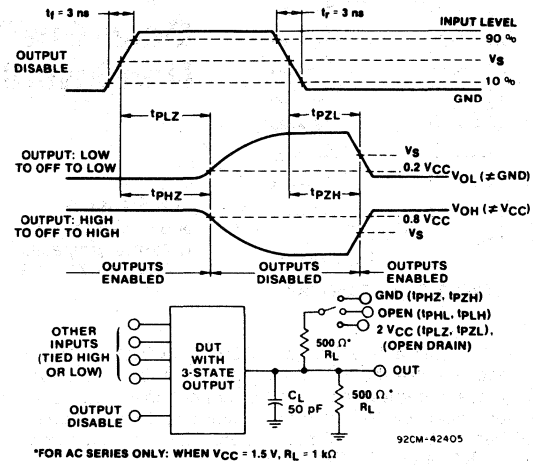
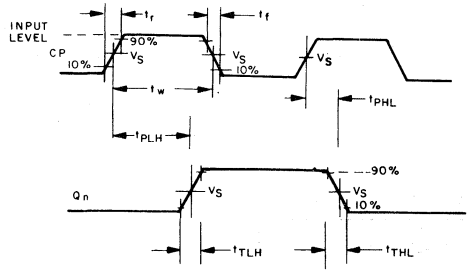


Fig. 2 - Three-state propagation delay waveforms and test circuit.



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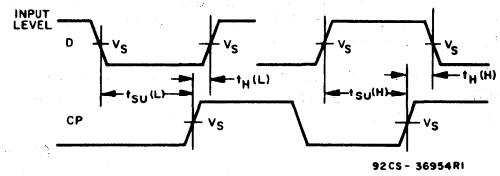

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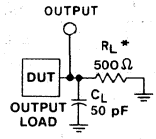

*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

92CS-42389

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Fig. 3 - Propagation delays times and test circuit.

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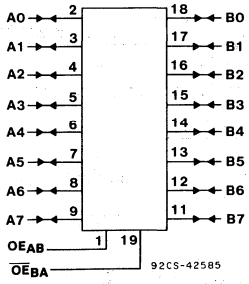
CD54/74AC623
CD54/74ACT623

Advance Information



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver, 3-State, Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  4.5 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA CD54/74AC623 and CD54/74ACT623 octal-bus transceivers use the RCA ADVANCED CMOS technology. They are non-inverting, 3-state, bidirectional transceiver-buffers that allow for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus, depending on the logic levels of the Output Enable (OE_{AB}, $\overline{OE}_{BA}$) inputs.

The dual Output Enable provision gives these devices the capability to store data by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input under these conditions, and when all other data sources to the bus lines are at high-impedance, both sets of bus lines will remain in their last states.

The CD74AC623 and CD74ACT623 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC623 and CD54ACT623, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

OUTPUT ENABLE INPUTS		OPERATION
$\overline{OE}_{BA}$	OE_{AB}	
L	L	B DATA TO A BUS
H	H	A DATA TO B BUS
H	L	ISOLATION
L	H	B DATA TO A BUS, A DATA TO B BUS

H = High level, L = Low level

Note: To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10 kΩ to 1 MΩ resistors.

File Number **1968**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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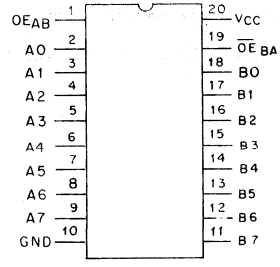

92CS-42586

TERMINAL ASSIGNMENT

CD54/74AC623
CD54/74ACT623

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL} #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
An, Bn	0.83
$\overline{OE}_{BA}$	0.64
OE_{AB}	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC623
CD54/74ACT623

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	t_{PLH} t_{PHL}	1.5 3.3* 5†	— 3.5 2.5	108 12.2 8.7	— 3.4 2.4	120 13.4 9.6	ns
Output Disable to Output	t_{PLZ} t_{PHZ}	1.5 3.3 5	— 4.8 3.5	153 17.1 12.2	— 4.7 3.4	168 18.8 13.4	ns
Output Enable to Output	t_{PZL} t_{PZH}	1.5 3.3 5	— 4.8 3.5	153 17.1 12.2	— 4.7 3.4	168 18.8 13.4	ns
Power Dissipation Capacitance	C_{PD}§	—	66 Typ.		66 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output	t_{PLH} t_{PHL}	5†	2.7	9.6	2.7	10.6	ns
Output Disable to Output	t_{PLZ} t_{PHZ}	5	3.7	13.1	3.6	14.4	ns
Output Enable to Output	t_{PZH} t_{PZL}	5	3.7	13.1	3.6	14.4	ns
Power Dissipation Capacitance	C_{PD}§	—	66 Typ.		66 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

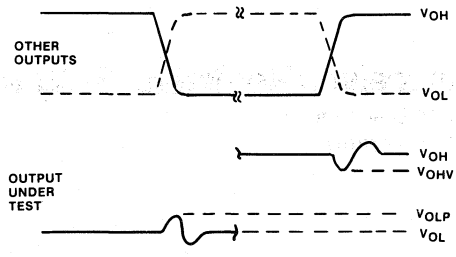
*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per channel.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC623
CD54/74ACT623

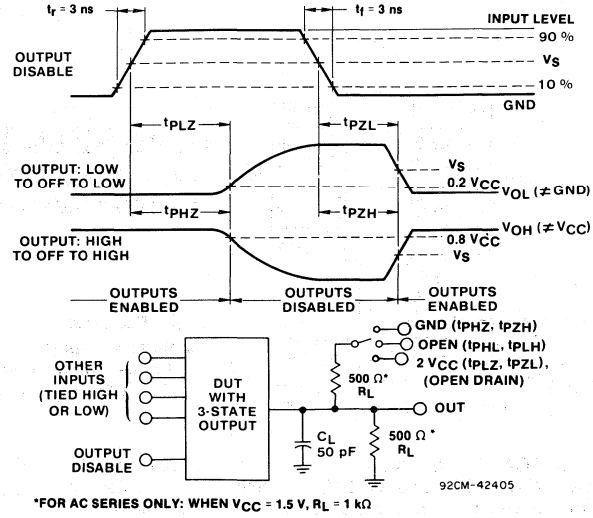
PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

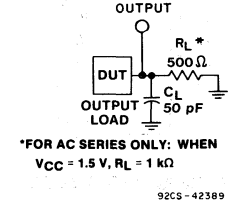
92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



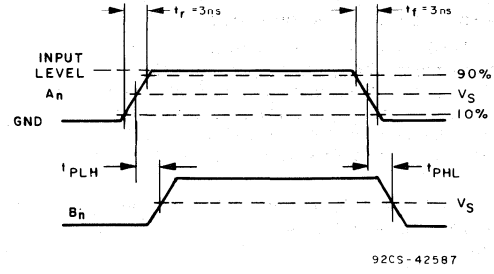
*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 2 - Three-state propagation delay times and test circuit.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

92CS-42389



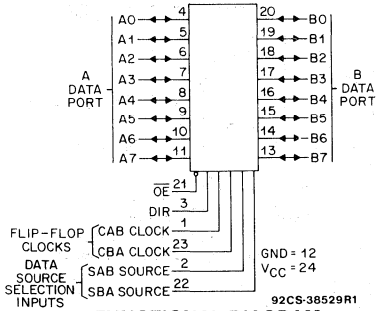
92CS-42587

Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

Advance Information



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver/Registers, 3-State

CD54/74AC/ACT646 - Non-Inverting
CD54/74AC/ACT648 - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  5.3 ns @ V_{CC} = 5 V, T_A = 25° C, C_L = 50 pF

The RCA CD54/74AC646 and CD54/74AC648 and the CD54/74ACT646 and CD54/74ACT648 3-state, octal-bus transceiver/registers use the RCA ADVANCED CMOS technology. The CD54/74AC648 and CD54/74ACT648 have inverting outputs. The CD54/74AC646 and CD54/74ACT646 have non-inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ($\overline{OE}$) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

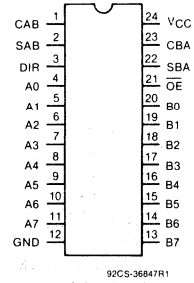
The CD74AC/ACT646 and CD74AC/ACT648 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 o +125°C).

The CD54AC/ACT646 and CD54AC/ACT648, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - Fanout to 15 FAST ICs*
  - Drives 50-ohm transmission lines

**FAST is a Registered Trademark of Fairchild Semiconductor Corp.*



TERMINAL ASSIGNMENT

File Number **1970**

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	646	648
X	X	↓	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↓	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↓	↓	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

#The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10 kΩ resistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
DIR	0.67
$\overline{OE}$	1.17
An, Bn	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f_{max}	1.5	11	—	10	—	MHz
		3.3*	101	—	89	—	
		5†	143	—	125	—	
Setup Time Data to Clock	t_{SU}	1.5	27	—	31	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
Hold Time Data to Clock	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Clock Pulse Width	t_W	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	

*3.3 V: min. is @ 3 V
†5 V: min is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:							
Store A Data to B Bus	t_{PLH}	1.5	—	154	—	169	ns
Store B Data to A Bus		3.3*	4.8	17.1	4.7	18.9	
646	t_{PHL}	5†	3.5	12.3	3.4	13.5	
Store $\overline{A}$ Data to B Bus	t_{PLH}	1.5	—	154	—	169	ns
Store $\overline{B}$ Data to A Bus		3.3	4.8	17.1	4.7	18.9	
648	t_{PHL}	5	3.5	12.3	3.4	13.5	
A Data to B Bus	t_{PLH}	1.5	—	125	—	138	ns
B Data to A Bus		3.3	4	14	3.9	15.4	
646	t_{PHL}	5	2.8	10	2.8	11	
$\overline{A}$ Data to B Bus	t_{PLH}	1.5	—	125	—	138	ns
$\overline{B}$ Data to A Bus		3.3	4	14	3.9	15.4	
648	t_{PHL}	5	2.8	10	2.8	11	
Select to Data	t_{PLH}	1.5	—	136	—	150	ns
646		3.3	4.3	15.3	4.2	16.8	
	t_{PHL}	5	3.1	10.9	3	12	
Select to Data	t_{PLH}	1.5	—	136	—	150	ns
648		3.3	4.3	15.3	4.2	16.8	
	t_{PHL}	5	3.1	10.9	3	12	
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	1.5	—	154	—	169	ns
		3.3	5.2	18.4	5.1	20.2	
		5	3.5	12.3	3.4	13.5	
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V
†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma (V_{CC}^2 C_L f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f_{max}	5*	125	—	110	—	MHz
Setup Time Data to Clock	t_{SU}	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t_H	5	2	—	2	—	ns
Clock Pulse Width	t_W	5	3.9	—	4.5	—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus, Store B Data to A Bus — 646	t_{PLH} t_{PHL}	5*	4	14.1	3.9	15.5	ns
Store $\overline{A}$ Data to B Bus, Store $\overline{B}$ Data to A Bus — 648	t_{PLH} t_{PHL}	5	4	14.1	3.9	15.5	ns
A Data to B Bus, B Data to A Bus — 646	t_{PLH} t_{PHL}	5	3.2	11.4	3.1	12.5	ns
$\overline{A}$ Data to B Bus, $\overline{B}$ Data to A Bus — 648	t_{PLH} t_{PHL}	5	3.2	11.4	3.1	12.5	ns
Select to Data — 646	t_{PLH} t_{PHL}	5	3.7	13.2	3.6	14.5	ns
Select to Data — 648	t_{PLH} t_{PHL}	5	4	14.1	3.9	15.5	ns
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o) + V_{CC}\Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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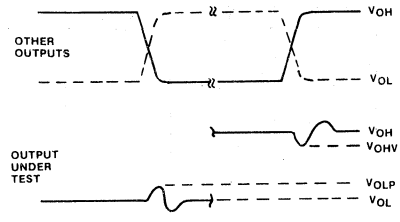
CD54/74AC646, CD54/74AC648
CD54/74ACT646, CD54/74ACT648

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.

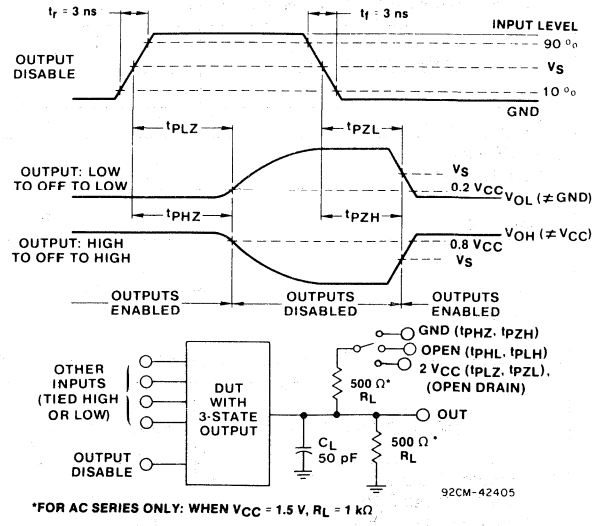


Fig. 2 - Three-state propagation delay waveforms and test circuit.

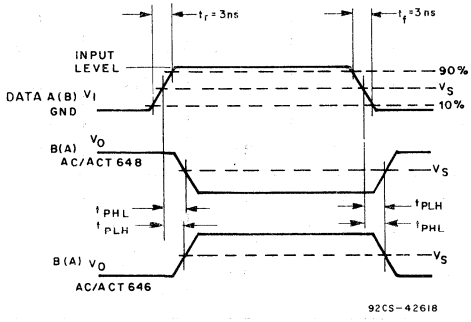


Fig. 3 - Propagation delay times.

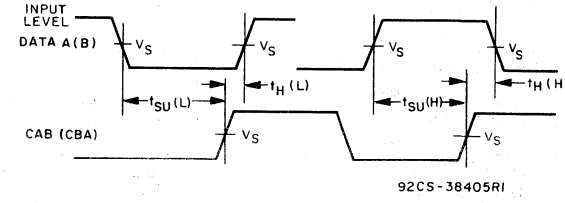


Fig. 4 - Data setup and hold times.

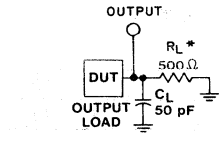
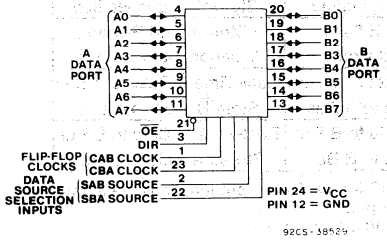


Fig. 5 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Advance Information

CD54/74AC647, CD54/74AC649
CD54/74ACT647, CD54/74ACT649



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver/Registers, with Open Drain

CD54/74AC/ACT647 - Non-Inverting
CD54/74AC/ACT649 - Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 7 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

Family Features:

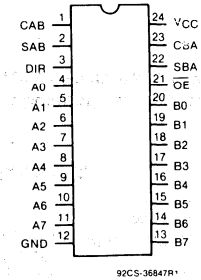
- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

The RCA CD54/74AC647 and CD54/74AC649 and the CD54/74ACT647 and CD54/74ACT649 open-drain, octal-bus transceiver/registers use the RCA ADVANCED CMOS technology. The CD54/74AC649 and CD54/74ACT649 have inverting outputs. The CD54/74AC647 and CD54/74ACT647 have non-inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ($\overline{OE}$) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

The CD74AC/ACT647 and CD74AC/ACT649 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT647 and CD54AC/ACT649, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.



TERMINAL ASSIGNMENT

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File Number **1982**

CD54/74AC647, CD54/74AC649
CD54/74ACT647, CD54/74ACT649

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
$\overline{OE}$	DIR	CAB	CBA	SAB	SBA	AD THRU A7	B0 THRU B7	647	649
X	X	↓	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↓	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↓	↓	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Store $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

#The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10 kΩ resistors.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
(For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC647, CD54/74AC649
CD54/74ACT647, CD54/74ACT649

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
Low-Level Output Voltage V_{OL}	V_{OL} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Off-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC647, CD54/74AC649
CD54/74ACT647, CD54/74ACT649

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
Low-Level Output Voltage V_{OL}	V_{OL} or V_{IL} #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Off-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
DIR	0.67
$\overline{OE}$	1.17
An, Bn	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC647, CD54/74AC649
CD54/74ACT647, CD54/74ACT649

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f_{max}	1.5	11	—	10	—	MHz
		3.3*	101	—	89	—	
		5†	143	—	125	—	
Setup Time Data to Clock	t_{SU}	1.5	15.8	—	18	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
Hold Time Data to Clock	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Clock Pulse Width	t_W	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	

*3.3 V: min. is @ 3 V
†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Stored A Data to B Bus 647, Stored $\overline{B}$ Data to A Bus 647, Stored $\overline{A}$ Data to B Bus 649, Stored $\overline{B}$ Data to A Bus 649	t_{PZL}	1.5	—	154	—	169	ns
		3.3*	5.2	18.4	5.1	20.2	
		5†	3.5	12.3	3.4	13.5	
	t_{PLZ}	1.5	—	166	—	183	ns
		3.3	4.7	18.6	4.6	18.3	
		5	3.8	13.3	3.7	14.6	
A Data to B Bus 647, $\overline{B}$ Data to A Bus 647, $\overline{A}$ Data to B Bus 649, $\overline{B}$ Data to A Bus 649	t_{PZL}	1.5	—	125	—	138	ns
		3.3	4.2	15	4.1	16.5	
		5	2.8	10	2.8	11	
	t_{PLZ}	1.5	—	137	—	151	ns
		3.3	3.9	13.7	3.8	15.1	
		5	3.1	11	3	12.1	
Select to Data 647, 649	t_{PZL}	1.5	—	136	—	150	ns
		3.3	4.6	16.4	4.5	18	
		5	3.1	10.9	3	12	
	t_{PLZ}	1.5	—	149	—	164	ns
		3.3	4.2	14.9	4.6	16.4	
		5	3.4	11.9	3.3	13.1	
Enable, Disable Times Bus to Output or Register to Output	t_{PZL} t_{PLZ}	1.5	—	154	—	169	ns
		3.3	5.2	18.4	5.1	20.2	
		5	3.5	12.3	3.4	13.5	
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
Off-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC647, CD54/74AC649
CD54/74ACT647, CD54/74ACT649

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f_{max}	5*	125	—	110	—	MHz
Setup Time Data to Clock	t_{SU}	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t_H	5	2	—	2	—	ns
Clock Pulse Width	t_W	5	3.9	—	4.5	—	ns

*5 V: min. is @ 4.5 V

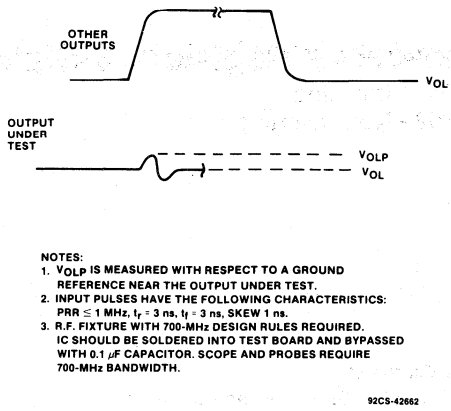
SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Stored A Data to B Bus / Stored $\overline{B}$ Data to A Bus (647)	t_{PZL}	5*	4	14.1	3.9	15.5	ns
Propagation Delays: Stored $\overline{A}$ Data to B Bus / Stored B Data to A Bus (649)	t_{PLZ}	5	4.3	15.1	4.2	16.6	ns
A Data to B Bus / $\overline{B}$ Data to A Bus (647)	t_{PZL}	5	3.2	11.4	3.1	12.5	ns
$\overline{A}$ Data to B Bus / B Data to A Bus (649)	t_{PLZ}	5	3.5	12.4	3.4	13.6	ns
Select to Data 647, 649	t_{PZL}	5	4	14.1	3.9	15.5	ns
	t_{PLZ}	5	4.3	15.1	4.2	16.6	ns
Enable, Disable Times Bus to Output or Register to Output	t_{PZL} t_{PLZ}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
Off-State Output Capacitance	C_O	—	—	15	—	15	pF

*5 V min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

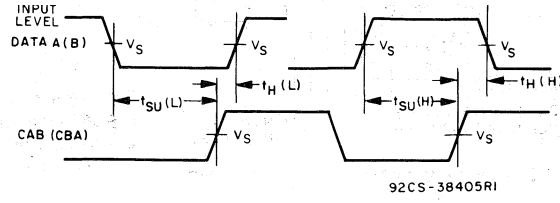
PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OLP} IS MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

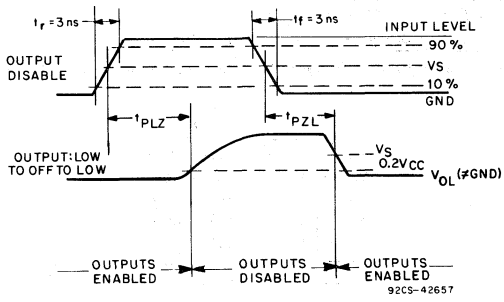
92CS-42662

Fig. 1 - Simultaneous switching transient waveforms.



92CS-38405RI

Fig. 2 - Data setup and hold times.



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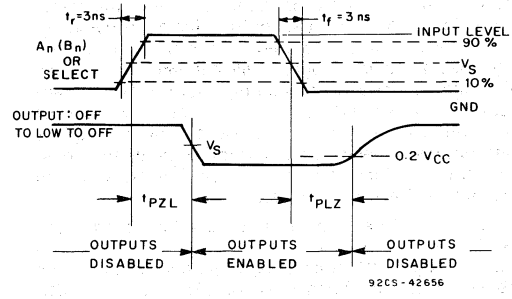

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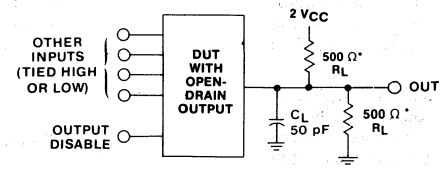

*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

92CS-42610

Fig. 3 - Open-drain propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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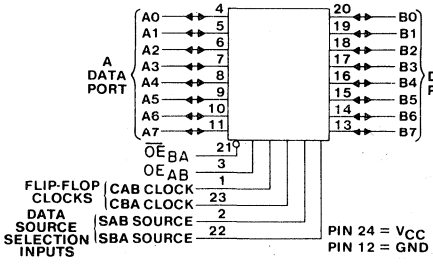
CD54/74AC651, CD54/74AC652
CD54/74ACT651, CD54/74ACT652

Advance Information



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver/Registers, 3-State

CD54/74AC/ACT651 - Inverting
CD54/74AC/ACT652 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  5.3 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA CD54/74AC651 and CD54/74AC652 and the CD54/74ACT651 and CD54/74ACT652 3-state, octal-bus transceiver/registers use the RCA ADVANCED CMOS technology. The CD54/74AC651 and CD54/74ACT651 have inverting outputs. The CD54/74AC652 and CD54/74ACT652 have non-inverting outputs. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OE_{AB} and $\overline{OE}_{BA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

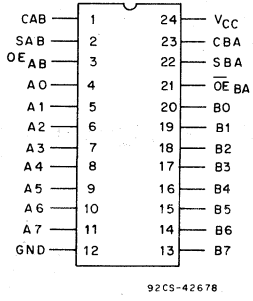
The CD74AC/ACT651 and CD74AC/ACT652 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT651 and CD54AC/ACT652, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 24-mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

**FAST is a Registered Trademark of Fairchild Semiconductor Corp.*



TERMINAL ASSIGNMENT

File Number **1974**

CD54/74AC651, CD54/74AC652
CD54/74ACT651, CD54/74ACT652

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OE_{AB}	$\overline{OE}_{BA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	651	652
L	H	H or L	H or L	X	X	Input	Input	Isolation *	Isolation*
L	H	⎍	⎍	X	X			Store A and B Data	Store A and B Data
X	H	⎍	H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H	⎍	⎍	X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	⎍	X	X	Unspecified†	Input	Hold A, Store B	Hold, A Store B
L	L	⎍	⎍	X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and	Stored A Data to B Bus
								Stored $\overline{B}$ Data to A bus	Stored B Data to A Bus

* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OE_{AB} or OE_{BA} inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

9

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
(For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC651, CD54/74AC652
CD54/74ACT651, CD54/74ACT652

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

CD54/74AC651, CD54/74AC652
CD54/74ACT651, CD54/74ACT652

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
		#, *	-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
		#, *	75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
OE_{AB}	0.67
$\overline{OE}_{BA}$	1.17
An, Bn	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC651, CD54/74AC652
CD54/74ACT651, CD54/74ACT652

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f_{max}	1.5	11	—	10	—	MHz
		3.3*	101	—	89	—	
		5†	143	—	125	—	
Setup Time Data to Clock	t_{SU}	1.5	27	—	31	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
Hold Time Data to Clock	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Clock Pulse Data to Clock	t_W	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	

*3.3 V: min. is @ 3 V
†5 V; min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus, Store B Data to A Bus — 652	t_{PLH} t_{PHL}	1.5	—	154	—	169	ns
		3.3*	4.8	17.1	4.7	18.9	
		5†	3.5	12.3	3.4	13.5	
Store $\overline{A}$ Data to B Bus, Store $\overline{B}$ Data to A Bus — 651	t_{PLH} t_{PHL}	1.5	—	154	—	169	ns
		3.3	4.8	17.1	4.7	18.9	
		5	3.5	12.3	3.4	13.5	
A Data to B Bus, B Data to A Bus — 652	t_{PLH} t_{PHL}	1.5	—	125	—	138	ns
		3.3	4	14	3.9	15.4	
		5	2.8	10	2.8	11	
$\overline{A}$ Data to B Bus, $\overline{B}$ Data to A Bus — 651	t_{PLH} t_{PHL}	1.5	—	125	—	138	ns
		3.3	4	14	3.9	15.4	
		5	2.8	10	2.8	11	
Select to Data — 652	t_{PLH} t_{PHL}	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
Select to Data — 651	t_{PLH} t_{PHL}	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	1.5	—	154	—	169	ns
		3.3	5.2	18.4	5.1	20.2	
		5	3.5	12.3	3.4	13.5	
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V
†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma (V_{CC}^2 C_L f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC651, CD54/74AC652
CD54/74ACT651, CD54/74ACT652

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f_{max}	5*	125	—	110	—	MHz
Setup Time Data to Clock	t_{SU}	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t_H	5	2	—	2	—	ns
Clock Pulse Width	t_W	5	3.9	—	4.5	—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus, Store B Data to A Bus — 652	t_{PLH} t_{PHL}	5*	4	14.1	3.9	15.5	ns
Store $\overline{A}$ Data to B Bus, Store $\overline{B}$ Data to A Bus — 651	t_{PLH} t_{PHL}	5	4	14.1	3.9	15.5	ns
A Data to B Bus, B Data to A Bus — 652	t_{PLH} t_{PHL}	5	3.2	11.4	3.1	12.5	ns
$\overline{A}$ Data to B Bus, $\overline{B}$ Data to A Bus — 651	t_{PLH} t_{PHL}	5	3.2	11.4	3.1	12.5	ns
Select to Data — 652	t_{PLH} t_{PHL}	5	3.7	13.2	3.6	14.5	ns
Select to Data — 651	t_{PLH} t_{PHL}	5	4	14.1	3.9	15.5	ns
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	15	—	15	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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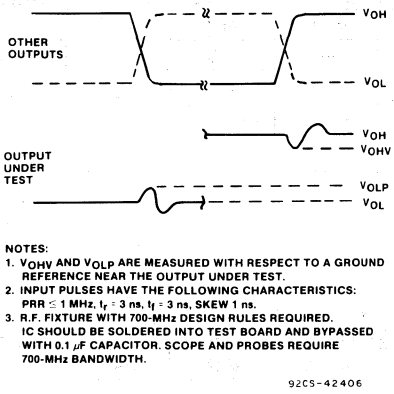
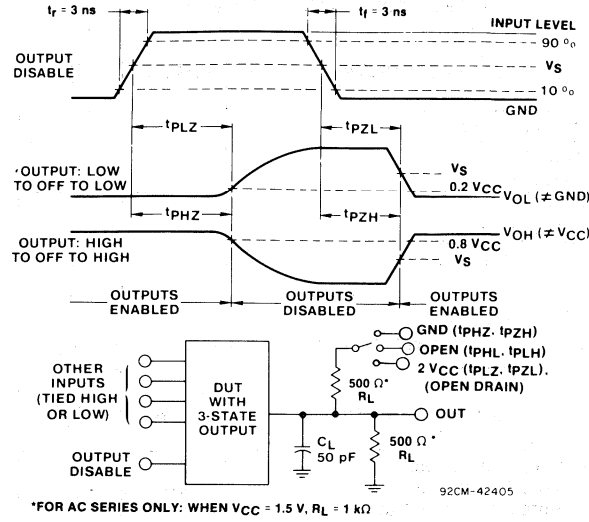
CD54/74AC651, CD54/74AC652
CD54/74ACT651, CD54/74ACT652



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 2 - Three-state propagation delay waveforms and test circuit.

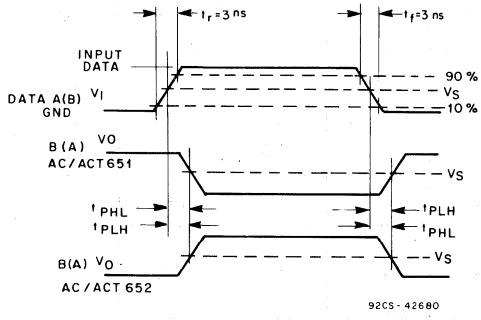


Fig. 3 - Propagation delay times.

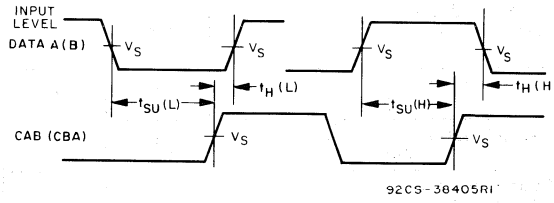
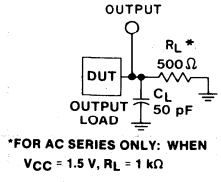


Fig. 4 - Data setup and hold times.



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

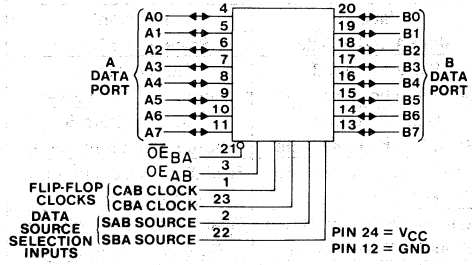
92CS-42389

Fig. 5 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Advance Information

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654



FUNCTIONAL DIAGRAM

Octal-Bus Transceivers/Registers, Open-Drain (A Side), 3-State (B Side)

CD54/74AC/ACT653 - Inverting
CD54/74AC/ACT654 - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 5.3 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF*

The RCA CD54/74AC653 and CD54/74AC654 and the CD54/74ACT653 and CD54/74ACT654 octal-bus transceivers/registers use the RCA ADVANCED CMOS technology. The CD54/74AC653 and CD54/74ACT653 are inverting types having open drains on the A outputs and 3-state outputs on the B side. The CD54/74AC654 and CD54/74ACT654 differ only in that these are non-inverting types. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OE_{AB} and $\overline{OE}_{BA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuit y used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

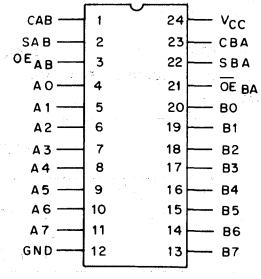
The CD74AC/ACT653 and CD74AC/ACT654 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT653 and CD54AC/ACT654, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latchup-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC types feature 1.5 V to 5.5 V operation and balanced noise immunity at 30% of the supply*
- *± 24 mA output drive current*
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.



TERMINAL ASSIGNMENT

9

File Number **1975**

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
OE_{AB}	$\overline{OE}_{BA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	653	654
L	H	H or L	H or L	X	X	Input	Input	Isolation *	Isolation*
L	H	⎍	⎍	X	X			Store A and B Data	Store A and B Data
X	H	⎍	H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H	⎍	⎍	X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	⎍	X	X	Unspecified†	Input	Hold A, Store B	Hold, A Store B
L	L	⎍	⎍	X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and	Stored A Data to B Bus and
								Stored $\overline{B}$ Data to A bus	Stored B Data to A Bus

* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OE_{AB} or $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
(For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
			3	2.1	—	2.1	—	2.1	—	
			5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage V_{IL}			1.5	—	0.3	—	0.3	—	0.3	V
			3	—	0.9	—	0.9	—	0.9	
			5.5	—	1.65	—	1.65	—	1.65	
High-Level Output Voltage (B Side) V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
	#, *	-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
	#, *	50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State or Off-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage (B Side) V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State or Off-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin, TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

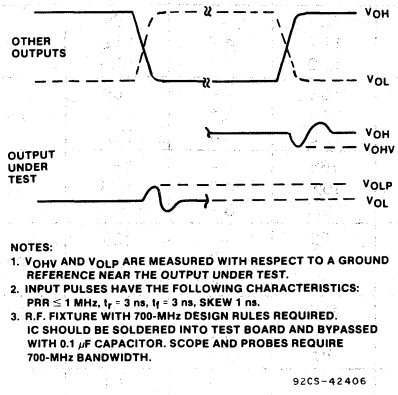
ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
$\overline{OE}_{AB}$	0.67
$\overline{OE}_{BA}$	1.17
An, Bn	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.

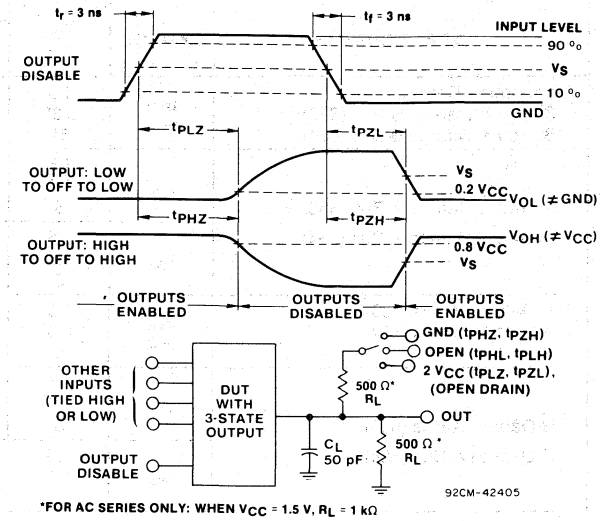


Fig. 2 - Three-state propagation delay waveforms and test circuit (B outputs).

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f_{max}	1.5	11	—	10	—	MHz
		3.3*	101	—	89	—	
		5†	143	—	125	—	
Setup Time Data to Clock	t_{SU}	1.5	27	—	31	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
Hold Time Data to Clock	t_H	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Clock Pulse Width Data to Clock	t_W	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	

* 3.3 V: min. is @ 3 V
† 5 V: min. is @ 4.5 V

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CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:		1.5	—	153	—	169	
Stored A Data to $\overline{B}$ Bus (653)	t_{PLH}	3.3*	4.9	17.2	4.7	18.9	ns
Stored A Data to B Bus (654)	t_{PHL}	5†	3.5	12.3	3.4	13.5	
		1.5	—	153	—	169	
	t_{PZL}	3.3	5.2	18.4	5.1	20.2	ns
Stored $\overline{B}$ Data to A Bus (653)		5	3.5	12.3	3.4	13.5	
Stored B Data to A Bus (654)		1.5	—	166	—	183	
	t_{PLZ}	3.3	4.7	16.6	4.6	18.3	ns
		5	3.8	13.3	3.7	14.6	
A Data to $\overline{B}$ Bus (653)		1.5	—	125	—	138	
A Data to B Bus (654)	t_{PLH}	3.3	4	14	3.9	15.4	ns
	t_{PHL}	5	2.8	10	2.8	11	
		1.5	—	125	—	138	
	t_{PZL}	3.3	4.2	15	4.1	16.5	ns
$\overline{B}$ Data to A Bus (653)		5	2.8	10	2.8	11	
B Data to A Bus (654)		1.5	—	137	—	151	
	t_{PLZ}	3.3	3.9	13.7	3.8	15.1	ns
		5	3.1	11	3	12.1	
Select to Data (B Bus)		1.5	—	136	—	150	
(653/654)	t_{PLH}	3.3	4.3	15.3	4.2	16.8	ns
	t_{PHL}	5	3.1	10.9	3	12	
		1.5	—	136	—	150	
	t_{PZL}	3.3	4.6	16.4	4.5	18	ns
Select to Data (A Bus)		5	3.1	10.9	3	12	
(653/654)		1.5	—	149	—	164	
	t_{PLZ}	3.3	4.2	14.9	4.1	16.4	ns
		5	3.4	11.9	3.3	13.1	
3-State Enabling/	t_{PZL}	1.5	—	154	—	169	
Disabling Time (B Bus)	t_{PZH}	3.3	5.2	18.4	5.1	20.2	ns
Bus to Output or	t_{PLZ}	5	3.5	12.3	3.4	13.5	
Register to Output (653/654)	t_{PHZ}						
Off-State Enabling/	t_{PZL}	1.5	—	154	—	169	
Disabling Time (A Bus)	t_{PLZ}	3.3	5.2	18.4	5.1	20.2	ns
Bus to Output or		5	3.5	12.3	3.4	13.5	
Register to Output (653/654)							
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Min. (Valley) V_{OH} (B Side)	V_{OHV}						
During Switching of Other Outputs	See	5	4 Typ. @ 25°C				V
(Output Under Test No Switching)	Fig. 1						
Max. (Peak) V_{OL}	V_{OLP}						
During Switching of Other Outputs	See	5	1 Typ. @ 25°C				V
(Output Under Test Not Switching)	Fig. 1						
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	C_O	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	C_O	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma (V_{CC}^2 C_L f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f_{max}	5*	125	—	110	—	MHz
Setup Time Data to Clock	t_{SU}	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t_H	5	2	—	2	—	ns
Clock Pulse Width	t_W	5	3.9	—	4.5	—	ns

*5 V:min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Stored A Data to $\overline{B}$ Bus (653) Stored A Data to B Bus (654)	t_{PLH} t_{PHL}	5*	4	14.1	3.9	15.5	ns
Stored $\overline{B}$ Data to A Bus (653)	t_{PZL}	5	4	14.1	3.9	15.5	ns
Stored B Data to A Bus (654)	t_{PLZ}	5	4.3	15.1	4.2	16.6	ns
A Data to $\overline{B}$ Bus (653) A Data to B Bus (654)	t_{PLH} t_{PHL}	5	3.2	11.4	3.1	12.5	ns
$\overline{B}$ Data to A Bus (653)	t_{PZL}	5	3.2	11.4	3.1	12.5	ns
B Data to A Bus (654)	t_{PLZ}	5	3.5	12.4	3.4	13.6	ns
Select to Data (B Bus) (653)	t_{PLH}	5	4	14.1	3.9	15.5	ns
(654)	t_{PHL}		3.7	13.2	3.6	14.5	
Select to Data (A Bus) (653/654)	t_{PZL}	5	4	14.1	3.9	15.5	ns
	t_{PLZ}	5	4.3	15.1	4.2	16.6	ns
3-State Enabling/ Disabling Time (B Bus) Bus to Output or Register to Output (653/654)	t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	5	4	14.1	3.9	15.5	ns
Off-State Enabling/ Disabling Time (A Bus) Bus to Output or Register to Output (653/654)	t_{PZL} t_{PLZ}	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C_{PD}§	—	150 Typ.		150 Typ.		pF
Min. (Valley) V_{OH} (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	C_O	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	C_O	—	—	15	—	15	pF

* Min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

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CD54/74AC653, CD54/74AC654
CD54/74ACT653, CD54/74ACT654

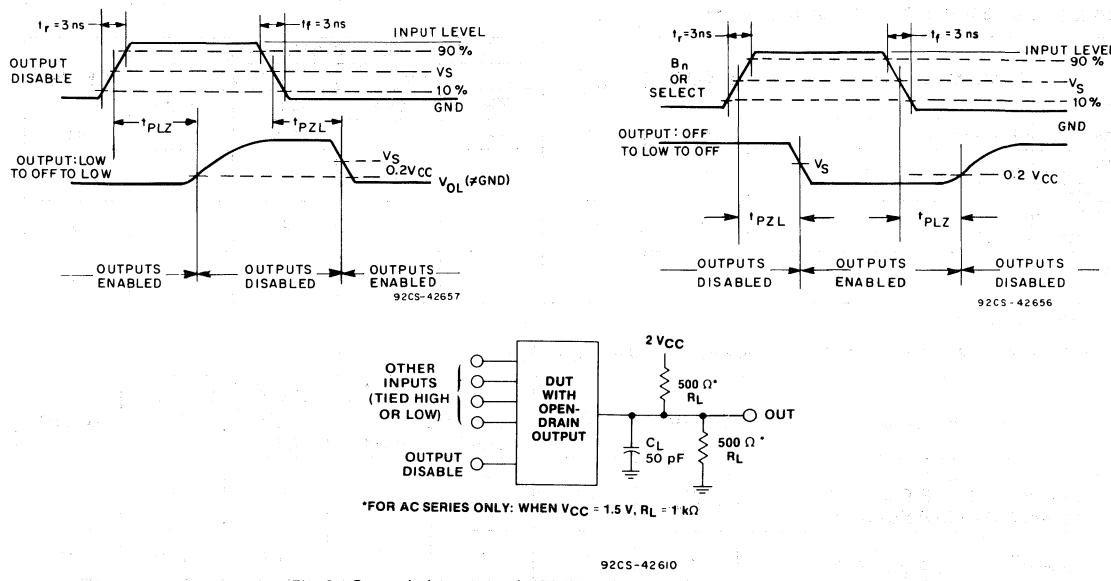


Fig. 3 - Open-drain propagation delay times and test circuit (A outputs).

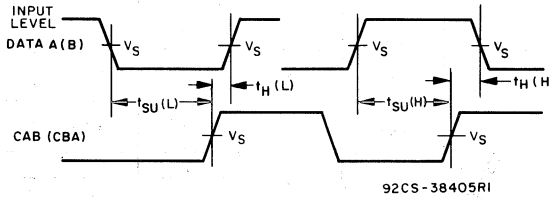
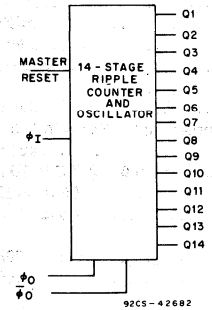


Fig. 4 - Data setup and hold times.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Advance Information

CD54/74AC7060, CD54/74AC7061
CD54/74ACT7060, CD54/74ACT7061



FUNCTIONAL DIAGRAM

14-Stage Binary Counter with Oscillator

Type Features:
- *On-board oscillator*
- *Buffered inputs*
- *Common reset*
- *Negative-edge clocking*
- *Typical f_{MAX} = 200 MHz @ V_{CC} = 5 V, C_L = 50 pF*
- *AC/ACT7060 Enabling Reset disables oscillator*
- *AC/ACT7061 oscillator continues to run when Reset is enabled*

The RCA-CD54/74AC7060 and CD54/74AC7061 and the CD54/74ACT7060 CD54/74ACT7061 each consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A Master Reset input is provided which resets the counter to the all-0's state and disables the oscillator in the 7060. In the 7061 the oscillator continues to run when the Master Reset is enabled. A high level on the MR line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in the binary order on the negative transition of ϕI (and ϕO). All inputs and outputs are buffered. Schmitt trigger action on the input-pulse line permits much slower rise and fall slew rates.

In order to achieve a symmetrical waveform in the oscillator section, the ACT7060 and 7061 input pulse switchpoints are the same as in the AC7060 and 7061 except the MR input in the ACT7060 and 7061 has TTL switching levels.

The CD74AC/ACT7060 and the CD74AC/ACT7061 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to +70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C). The CD54AC/ACT7060 and the CD54-AC/ACT7061, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:
- *Exceeds 2-kV ESD protection–MIL-STD-883, Method 3015*
- *SCR-latchup-resistant CMOS process and circuit design*
- *Balanced propagation delays*
- *AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply*
- *±24-mA output drive current* (Q1, Q2, and Q3)
  - *Fanout to 15 FAST* ICs*
  - *Drives 50-ohm transmission lines*

*FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

φI	MR	OUTPUT STATE
⌐‾	L	No Change
‾⌐	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)
L = low level (steady state)
X = don't care

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File Number **2062**

CD54/74AC7060, CD54/74AC7061
CD54/74ACT7060, CD54/74ACT7061

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC}$ +0.5 V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC}$ +0.5 V) ..... ±50 mA
DC V_{CC} OR GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPES E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into PC board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only ..... +300°C

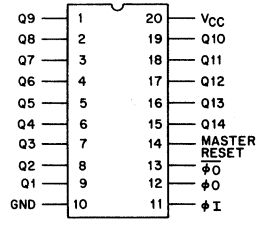
*(For up to 4 outputs per device; add ±25 mA for each additional output.)

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range	V_{CC}*			
(For T_A = Full Package-Temperature Range)				
AC Types		1.5	5.5	V
ACT Types		4.5	5.5	
DC Input or Output Voltage	V_I, V_O	0	V_{CC}	V
Operating Temperature	T_A	-55	+125	°C
Input Rise and Fall Slew Rate	dt/dv†			
at 1.5 V to 3 V (AC Types)		0	50	
at 3.6 V to 5.5 V (AC Types)		0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)		0	10	

†Applicable for MR. Schmitt input on ϕI line permits slower slew rates.
*Unless otherwise specified, all voltages are referenced to ground.



92CS-43092

TERMINAL ASSIGNMENT

CD54/74AC7060, CD54/74AC7061
CD54/74ACT7060, CD54/74ACT7061

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTIC		TEST CONDITIONS		V_{CC}	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V_I (V)	I_O (mA)	(V)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
Low-Level Input Voltage	V_{IL}			1.5	—	0.3	—	0.3	—	0.3	
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
Output High Voltage	V_{OH}	V_{IH}	-0.05	1.5	1.4	—	1.4	—	1.4	—	
All Outputs		or	-0.05	3	2.9	—	2.9	—	2.9	—	
		V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	
ϕ_0, $\overline{\phi_0}$		V_{IH}	-2	3	2.58	—	2.48	—	2.4	—	
		or									
(Pins 12, 13)		V_{IL}	-12	4.5	3.94	—	3.8	—	3.7	—	
Q1, Q2, Q3		V_{IH}	-4	3	2.58	—	2.48	—	2.4	—	
		or									
		V_{IL}	-24	4.5	3.94	—	3.8	—	3.7	—	
		#*	75	5.5	—	—	3.85	—	—	—	
		#*	50	5.5	—	—	—	—	3.85	—	
Q4 thru Q14		V_{IH}	-1.3	3	2.58	—	2.48	—	2.4	—	
		or									
		V_{IL}	-8	4.5	3.94	—	3.8	—	3.7	—	
Output Low Voltage	V_{OL}	V_{IH}	-0.05	1.5	—	0.1	—	0.1	—	0.1	
All Outputs		or	-0.05	3	—	0.1	—	0.1	—	0.1	
		V_{IL}	-0.05	4.5	—	0.1	—	0.1	—	0.1	
ϕ_0, $\overline{\phi_0}$		V_{IH}	6	3	—	0.36	—	0.44	—	0.50	
		or									
(Pins 12, 13)		V_{IL}	12	4.5	—	0.36	—	0.44	—	0.50	
Q1, Q2, Q3		V_{IH}	12	3	—	0.36	—	0.44	—	0.50	
		or									
		V_{IL}	24	4.5	—	0.36	—	0.44	—	0.50	
		#*	75	5.5	—	—	—	1.65	—	—	
		#*	50	5.5	—	—	—	—	—	1.65	
Q4 thru Q14		V_{IH}	4	3	—	0.36	—	0.44	—	0.50	
		or									
		V_{IL}	8	4.5	—	0.36	—	0.44	—	0.50	
Input Leakage Current	I_I	V_{CC}									
		or		5.5	—	±0.1	—	±1	—	±1	μA
		Gnd									
Quiescent Supply Current, MSI	I_{CC}	V_{CC}									
		or	0	5.5	—	8	—	80	—	160	
		Gnd									

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-Ω transmission-line-drive capability at +85°C, 75 ohms at +125°C.

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CD54/74AC7060, CD54/74AC7061
CD54/74ACT7060, CD54/74ACT7061

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTIC	TEST CONDITIONS		V_{CC}	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)	(V)	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH} MR Only			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL} MR Only			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
Output High Voltage V_{OH} All Outputs	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
ϕ_O, $\overline{\phi_O}$ (Pins 12, 13)	V_{IH} or V_{IL}	-12	4.5	3.94	—	3.8	—	3.7	—	V
Q1, Q2, Q3	V_{IH} or V_{IL}	-24	4.5	3.94	—	3.8	—	3.7	—	V
	#*	-75	5.5	—	—	3.85	—	—	—	V
	#*	-50	5.5	—	—	—	—	3.85	—	V
Q4 thru Q14	V_{IH} or V_{IL}	-8	4.5	3.94	—	3.8	—	3.7	—	V
Output Low Voltage V_{OL} All Outputs	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
ϕ_O, $\overline{\phi_O}$ (Pins 12, 13)	V_{IH} or V_{IL}	12	4.5	—	0.36	—	0.44	—	0.50	V
Q1, Q2, Q3	V_{IH} or V_{IL}	24	4.5	—	0.36	—	0.44	—	0.50	V
	#*	75	5.5	—	—	—	1.65	—	—	V
	#*	50	5.5	—	—	—	—	—	1.65	V
Q4 thru Q14	V_{IH} or V_{IL}	8	4.5	—	0.36	—	0.44	—	0.50	V
Input Leakage Current I_I	V_{CC} or Gnd		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or Gnd	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin, TTL Inputs High Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-Ω transmission-line-drive capability at +85° C, 75 ohms at +125° C.

CD54/74AC7060, CD54/74AC7061
CD54/74ACT7060, CD54/74ACT7061

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTIC		V_{CC} (V)	AMBIENT TEMPERATURE—°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Input Pulse Width	t_W	1.5	55	—	63	—	ns
		3.3*	6.1	—	7	—	
		5†	4.4	—	5	—	
Reset Pulse Width	t_W	1.5	44	—	50	—	
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	
Reset Removal Time	t_{REM}	1.5	44	—	50	—	
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	
Minimum Input Pulse Frequency	f_{MAX}	1.5	9.1	—	8	—	MHz
		3.3	81	—	71	—	
		5	114	—	100	—	

*3.3 V: min. is @ 3 V.
†5 V: min. is @ 4.5 V.

SWITCHING CHARACTERISTICS: AC Series, t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTIC		V_{CC} (V)	AMBIENT TEMPERATURE—°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays:	t_{PLH}	1.5	—	230	—	254	ns
ϕI to Q1	t_{PHL}	3.3*	7.2	25	7	28	
		5†	5.3	18.5	5.1	20.3	
	t_{PLH}	1.5	—	68	—	75	
Qn to Qn + 1	t_{PHL}	3.3	2.2	7.6	2.1	8.4	
		5	1.5	5.5	1.5	6	
	t_{PLH}	1.5	—	262	—	288	
MR to Qn	t_{PHL}	3.3	8.3	29.3	8.1	32.2	
		5	6	21	5.8	23	
Power Dissipation Capacitance	C_{PD}§	—	114 Typ.		114 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	

*3.3 V: min. is @ 3.6 V
max. is @ 3 V
†5 V: min. is @ 5.5 V
max. is @ 4.5 V
§C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$P_D = C_{PD}V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTIC		V_{CC} (V)	AMBIENT TEMPERATURE—°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Input Pulse Width	t_W	5*	4.4	—	5	—	ns
Reset Pulse Width	t_W	5	3.5	—	4	—	
Reset Removal Time	t_{REM}	5	4.4	—	5	—	
Minimum Input Pulse Frequency	f_{MAX}	5	114	—	100	—	MHz

*Min. is @ 4.5 V.

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CD54/74AC7060, CD54/74AC7061
CD54/74ACT7060, CD54/74ACT7061

SWITCHING CHARACTERISTICS: ACT Series, t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTIC		V_{CC} (V)	AMBIENT TEMPERATURE—°C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: ϕI to Q1	t_{PLH} / t_{PHL}	5*	5.3	18.5	5.1	20.3	ns
Qn to Qn + 1	t_{PLH} / t_{PHL}	5	1.5	5.5	1.5	6	ns
MR to Qn	t_{PLH} / t_{PHL}	5	6.3	22.1	6.1	24.3	ns
Power Dissipation Capacitance	C_{PD}§	—	114 Typ.		114 Typ.		pF
Input Capacitance	C_I	—	—	10	—	10	pF

*Min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per flip-flop.

$P_D = C_{PD}V_{CC}^2f_i + \Sigma (C_LV_{CC}^2f_o) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

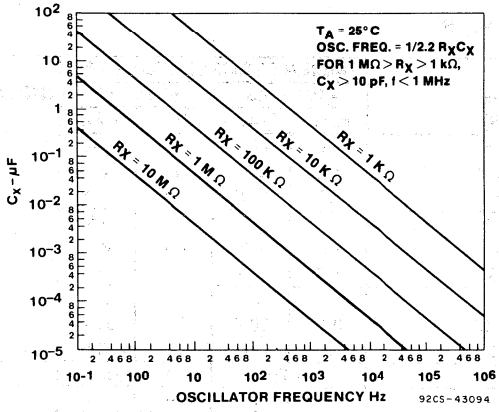


Fig. 1 - Frequency on on-board oscillator as a function of C_X and R_X.

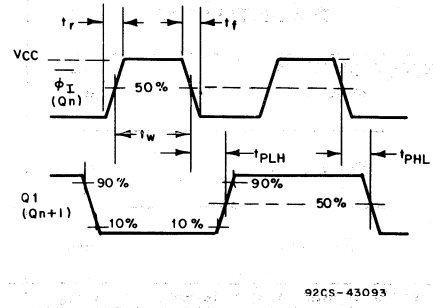
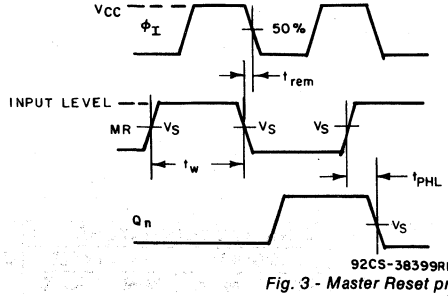


Fig. 2 - Input pulse pre-requisite times and propagation delays for both AC and ACT types.



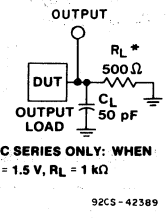
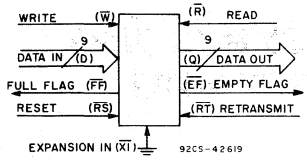


Fig. 3 - Master Reset pre-requisite and propagation delays.

	CD54/74AC	CD54/74ACT
MR Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

Product Preview

CD54/74AC7201, CD54/74AC7202
CD54/74ACT7201, CD54/74ACT7202



FUNCTIONAL DIAGRAM

Parallel FIFO

CD54/74AC/ACT7201 - 512 x 9 Bit
CD54/74AC/ACT7202 - 1024 x 9 Bit

Type Features:

- *Asynchronous and simultaneous read/writes in multiprocessing and rate-buffer applications*
- *Fully expandable by both word depth and/or bit width*

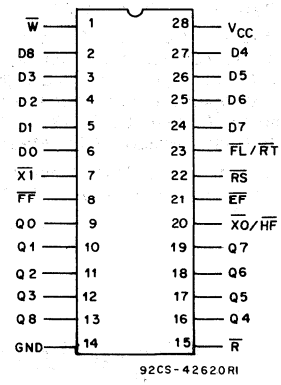
The RCA CD54/74AC7201 and CD54/74AC7202 and the CD54/74ACT7201 and CD54/74ACT7202 dual-port memories use the RCA ADVANCED CMOS technology. Data are loaded and emptied on a first-in, first-out (FIFO) basis. Full and empty flags are used to prevent data overflow and underflow, and expansion logic is provided for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers; no address information is required to load and unload data. Data are toggled in and out of the device through the use of Write ($\overline{W}$) and Read ($\overline{R}$) control pins.

The 9-bit wide data array allows control and parity bits to be used at the user's option. This device also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed LOW to allow for transmission from the beginning of data.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Balanced propagation delays*
- *AC type features 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply*
- *± 8 mA output drive current*



TERMINAL ASSIGNMENT

TRUTH TABLE

RESET AND RETRANSMIT — SINGLE-DEVICE CONFIGURATION/WIDTH-EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset	0	X	0	Location Zero	Location Zero	0	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X
Read/Write	1	1	0	Increment*	Increment*	X	X

*Pointer will increment if flag is HIGH.

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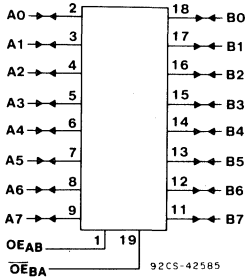
CD54/74AC7623
CD54/74ACT7623

Advance Information



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver, 3-State (B Side), Open-Drain (A Side), Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay:*
  5.2 ns @ V_{CC} = 5 V, T_A = 25°C, C_L = 50 pF

The RCA CD54/74AC7623 and CD54/74ACT7623 octal-bus transceivers use the RCA ADVANCED CMOS technology. They are non-inverting, 3-state, bidirectional transceiver-buffers that allow for two-way transmission from "A" bus to "B" bus or "B" bus to "A" bus, depending on the logic levels of the Output Enable (OE_{AB}, $\overline{OE}_{BA}$) inputs.

These devices are modified versions of the CD54/74AC/ACT623. They differ in that the 3-state outputs are on the B side only; the A side outputs are open drain. Another difference is that the A data inputs are TTL inputs for both the AC and ACT types, and therefore the supply-voltage and bus-voltage ranges are limited to 4.5 V to 5.5 V.

The CD74AC7623 and CD74ACT7623 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC7623 and CD54ACT7623, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

Family Features:

- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed of bipolar FAST*/AS/S with significantly reduced power consumption*
- *Balanced propagation delays*
- *AC type features balanced noise immunity at 30% of the supply on the B data inputs and Output Enable inputs*
- *± 24-mA output drive current*
  - Fanout to 15 FAST ICs*
  - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

OUTPUT ENABLE INPUTS		OPERATION
$\overline{OE}_{BA}$	OE_{AB}	
L	L	B DATA TO (OPEN DRAIN) A BUS
H	H	A DATA (TTL) TO (3-STATE) B BUS
H	L	ISOLATION
L	H	B DATA TO (OPEN DRAIN) A BUS, A DATA (TTL) TO (3-STATE) B BUS

H = High level, L = Low level

To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

File Number **1969**

CD54/74AC7623
CD54/74ACT7623

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*: (For T_A = Full Package-Temperature Range)			
AC Types	4.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 4.5 V to 5.5 V (AC Types Except B Inputs)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types and B Inputs)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

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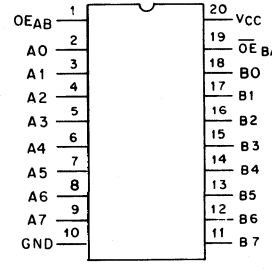

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TERMINAL ASSIGNMENT

CD54/74AC7623
CD54/74ACT7623

STATIC ELECTRICAL CHARACTERISTICS: AC Series (Modified)

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		-40 to +85		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage ■	V_{IH}			5.5	3.85	—	3.85	—	3.85	—	V
Low-Level Input Voltage ■	V_{IL}			5.5	—	1.65	—	1.65	—	1.65	V
High-Level Output Voltage (B Side)	V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		#, *	-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		#, *	24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State or Off-State Leakage Current	I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

■For "A" side V_{IH} and V_{IL}, refer to ACT limits.

CD54/74AC7623
CD54/74ACT7623

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage (B Side) V_{OH}	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
		-24	4.5	3.94	—	3.8	—	3.7	—	
	#, *	-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
		24	4.5	—	0.36	—	0.44	—	0.5	
	#, *	75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State or Off-State Leakage Current I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
An, Bn	0.83
$\overline{OE}_{BA}$	0.64
OE_{AB}	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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CD54/74AC7623
CD54/74ACT7623

SWITCHING CHARACTERISTICS: AC Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A Data to B Bus	t_{PLH} t_{PNL}	5*	2.8	9.9	2.7	10.9	ns
B Data to A Bus	t_{PZL}	5	2.5	8.7	2.4	9.6	ns
	t_{PLZ}	5	3.5	12.2	3.4	13.4	ns
Output Enable or Disable to Output 3-State (B Side)	t_{PZL} t_{PLZ} t_{PZH} t_{PHZ}	5	3.5	12.2	3.4	13.4	ns
Off-State Enabling, Disabling Times (A Side)	t_{PZL} t_{PLZ}	5	3.5	12.2	3.4	13.4	ns
Power Dissipation Capacitance	C_{PD}§	—	117 Typ.		117 Typ.		pF
Min. (Valley) V_{OH} (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	C_O	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	C_O	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

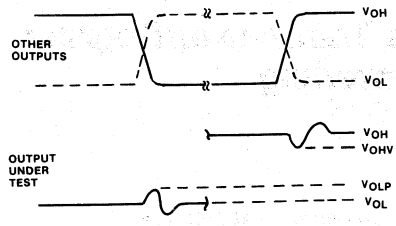
CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: A Data to B Bus	t_{PLH} t_{PHL}	5*	2.8	9.9	2.7	10.9	ns
B Data to A Bus	t_{PZL}	5	2.8	9.9	2.7	10.9	ns
	t_{PLZ}	5	3.8	13.4	3.7	14.7	ns
Output Enable or Disable to Output 3-State (B Side)	t_{PZH} t_{PZL} t_{PLZ} t_{PHZ}	5	3.8	13.4	3.7	14.7	ns
Off-State Enabling, Disabling Times (A Side)	t_{PZL} t_{PLZ}	5	3.8	13.4	3.7	14.7	ns
Power Dissipation Capacitance	C_{PD}§	—	117 Typ.		117 Typ.		pF
Min. (Valley) V_{OH} (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_I	—	—	10	—	10	pF
3-State Output Capacitance (B Side)	C_O	—	—	15	—	15	pF
Off-State Output Capacitance (A Side)	C_O	—	—	15	—	15	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per channel.
For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage.

CD54/74AC7623
CD54/74ACT7623

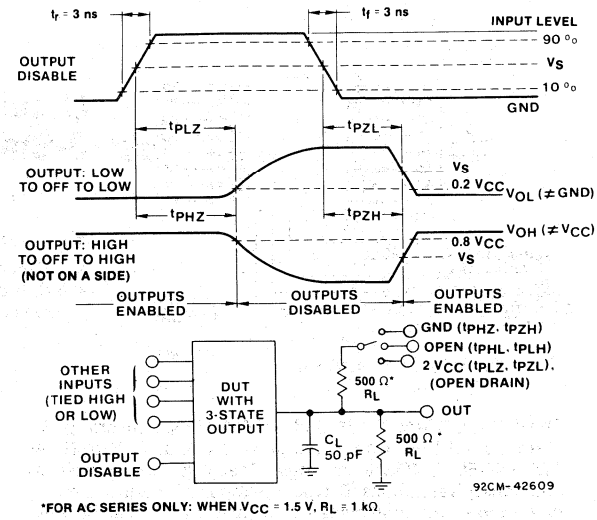
PARAMETER MEASUREMENT INFORMATION



NOTES:
1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, t_r = 3 ns, t_f = 3 ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μF CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

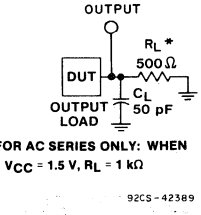
92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



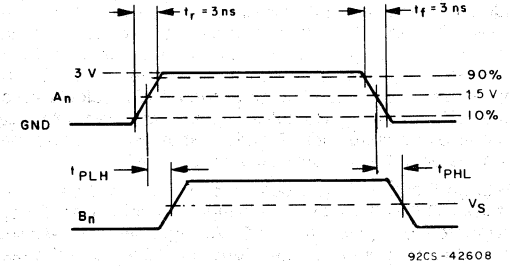
*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

Fig. 2 - Three-state propagation delay times and test circuit.



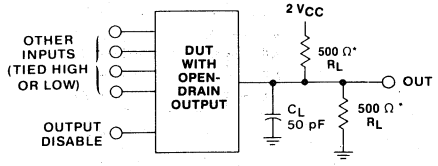
*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

92CS-42389



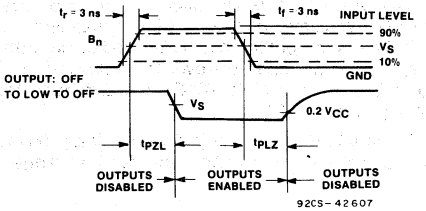
92CS-42608

Fig. 3 - Propagation delay times and test circuit (A Data to B Bus).



*FOR AC SERIES ONLY: WHEN V_{CC} = 1.5 V, R_L = 1 kΩ

92CS-42610



92CS-42607

Fig. 4 - Open-drain propagation delay times and test circuit (B Data to A Outputs).

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

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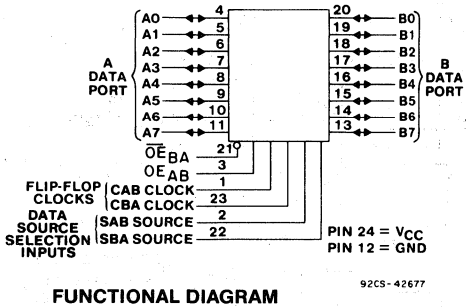
CD54/74ACT7651

Advance Information



FUNCTIONAL DIAGRAM

Octal-Bus Transceiver/Register, 3-State, Inverting

Type Features:

- *Buffered inputs*
- *B Side drive is equivalent to the ALS651 type (see application, Fig. 6)*

Family Features:

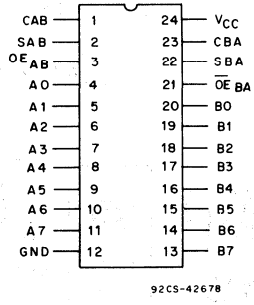
- *Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015*
- *SCR-Latch-up-resistant CMOS process and circuit design*
- *Speed exceeding bipolar ALSTTL with significantly reduced power consumption*

The RCA CD54ACT7651 and CD74ACT7651 inverting, 3-state, octal-bus transceivers/registers use the RCA ADVANCED CMOS technology. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OE_{AB} and $\overline{OE}_{BA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OE_{AB} and $\overline{OE}_{BA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The CD74ACT7651 is supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C) and Extended Industrial/ Military (-55 to +125°C).

The CD54ACT7651, available in chip form (H suffix), is operable over the -55 to +125°C temperature range.



TERMINAL ASSIGNMENT

File Number **2196**

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	
L	H	H or L	H or L	X	X	Input	Input	Isolation *
L	H	⎍	⎍	X	X			Store A and B Data
X	H	⎍	H or L	X	X	Input	Unspecified†	Store A, Hold B
H	H	⎍	⎍	X‡	X	Input	Output	Store A in both registers
L	X	H or L	⎍	X	X	Unspecified†	Input	Hold A, Store B
L	L	⎍	⎍	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A bus

* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OE_{AB} or $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.
Select control = H: clocks must be staggered in order to load both registers.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE EN) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE EN) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

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RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}* (For T_A = Full Package-Temperature Range)	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

CD54/74ACT7651

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		0 to +70		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
	Side A	or	-6	4.5	3.4	—	3.2	—	3	—	
	Side B	V_{IL}	-12	4.5	3.4	—	3.2	—	3	—	
Low-Level Output Voltage	V_{OL}	V_{IH}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
	Side A	or	12	4.5	—	0.36	—	0.44	—	0.5	
	Side B	V_{IL}	24	4.5	—	0.36	—	0.44	—	0.5	—
Input Leakage Current	I_I	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
3-State Leakage Current	I_{OZ}	V_{IH} or V_{IL} V_O = V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
OE_{AB}	0.67
$\overline{OE}_{BA}$	1.17
An, Bn	0.4

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

PREREQUISITE FOR SWITCHING: ACT Series

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			0 to +70		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Maximum Frequency	f_{max}	5*	125	—		—	MHz
Setup Time Data to Clock	t_{SU}	5	2.2	—		—	ns
Hold Time Data to Clock	t_H	5	2	—		—	ns
Clock Pulse Width	t_W	5	3.9	—		—	ns

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_r, t_f = 3 ns, C_L = 50 pF

CHARACTERISTICS		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
				0 to +70		-55 to +125		
				MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Stored A Data to B Bus		t_{PHL}	5*	4.2	12.6			ns
		t_{PLH}		5.4	16.1			
Stored B Data to A Bus		t_{PHL}	5	4.5	13.5			ns
		t_{PLH}		7.6	22.7			
A Data to B Bus		t_{PHL}	5	3.8	11.4			ns
		t_{PLH}		4.8	14.3			
B Data to A Bus		t_{PHL}	5	3.8	11.4			ns
		t_{PLH}		6.8	20.3			
Select to B Bus		t_{PHL}	5	4.2	12.5			ns
		t_{PLH}		5.3	15.8			
Select to A Bus		t_{PHL}	5	4.3	12.8			ns
		t_{PLH}		7.3	21.9			
3-State Enabling Time Bus to Output or Register to Output	B Bus	t_{PZH}	5	5.1	15.3			ns
		t_{PZL}		3.8	11.4			
	A Bus	t_{PZH}		7.9	23.6			
		t_{PZL}		4.9	14.7			
3-State Enabling Time Bus to Output or Register to Output	B Bus	t_{PHZ}	5	3.8	11.3			ns
		t_{PLZ}		4.4	13.2			
	A Bus	t_{PHZ}		11.7	35†			
		t_{PLZ}		3.7	11			
Power Dissipation Capacitance		C_{PD}§	—	150 Typ.				pF
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV} See Fig. 2	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP} See Fig. 2	5	1 Typ @ 25°C				V
Input Capacitance		C_I	—	—	10	—	10	pF
3-State Output Capacitance		C_O	—	—	15	—	15	pF

* 5 V: min. is @ 5.5 V
max. is @ 4.5 V

§C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 C_{PD} f_i + \Sigma V_{CC}^2 C_L f_o + V_{CC} \Delta I_{CC}$ where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

† t_{PHZ} is measured at a fixed 3.0 V as shown in Fig. 1b. V_{OH} can range up to 4.0 V. The 35-ns maximum limit accounts for a fairly large variation due to the test method. In applications, t_{PHZ} is typically 15 ns.

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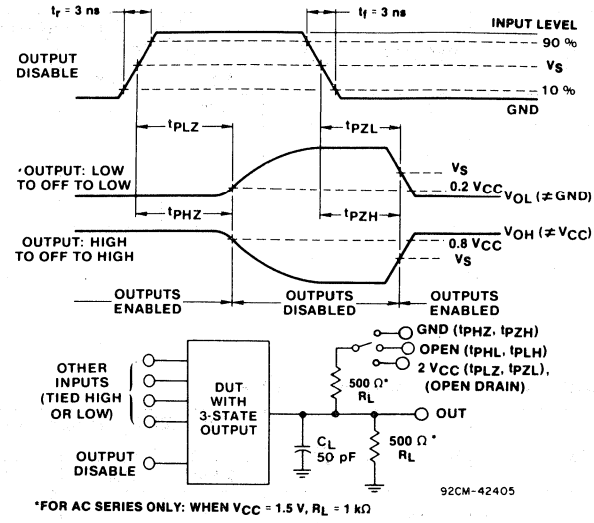
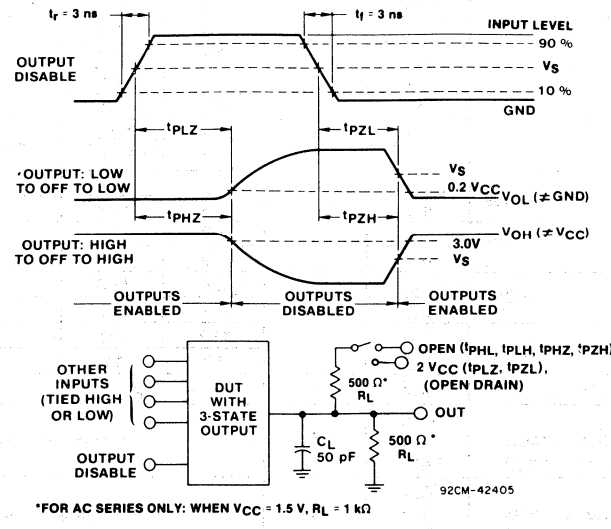
CD54/74ACT7651



(a)

Applicable to: B Bus - t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}



(b)

Applicable to: A Bus - t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

Fig. 1 - Three-state propagation delay times and test circuit.

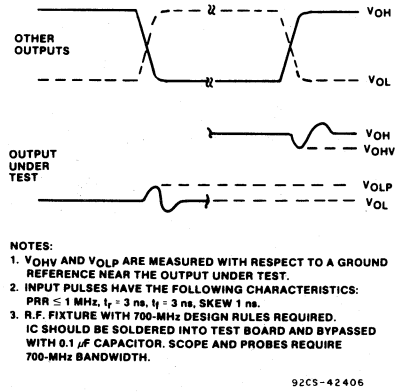


Fig. 2 - Simultaneous switching transient waveforms.

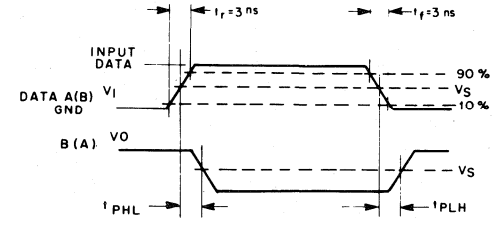


Fig. 3 - Propagation delay times.

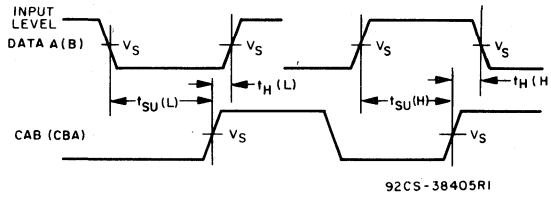


Fig. 4 - Data setup and hold times.

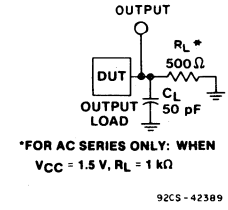


Fig. 5 - Test circuit.

	CD54/74ACT
Input Level	3 V
Input Switching Voltage, V_S	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}

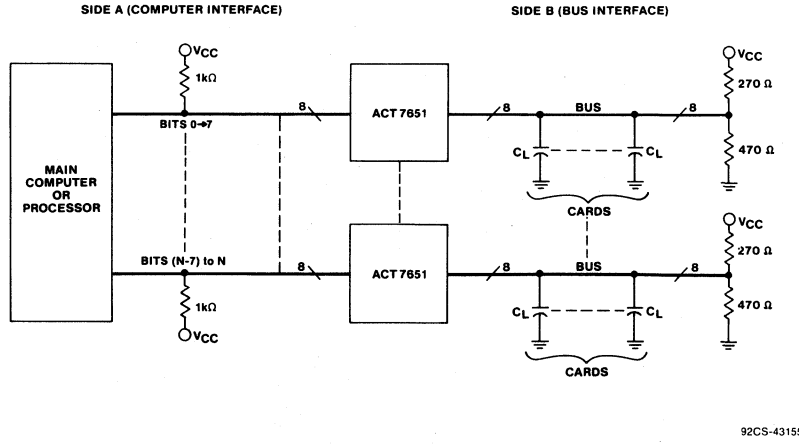
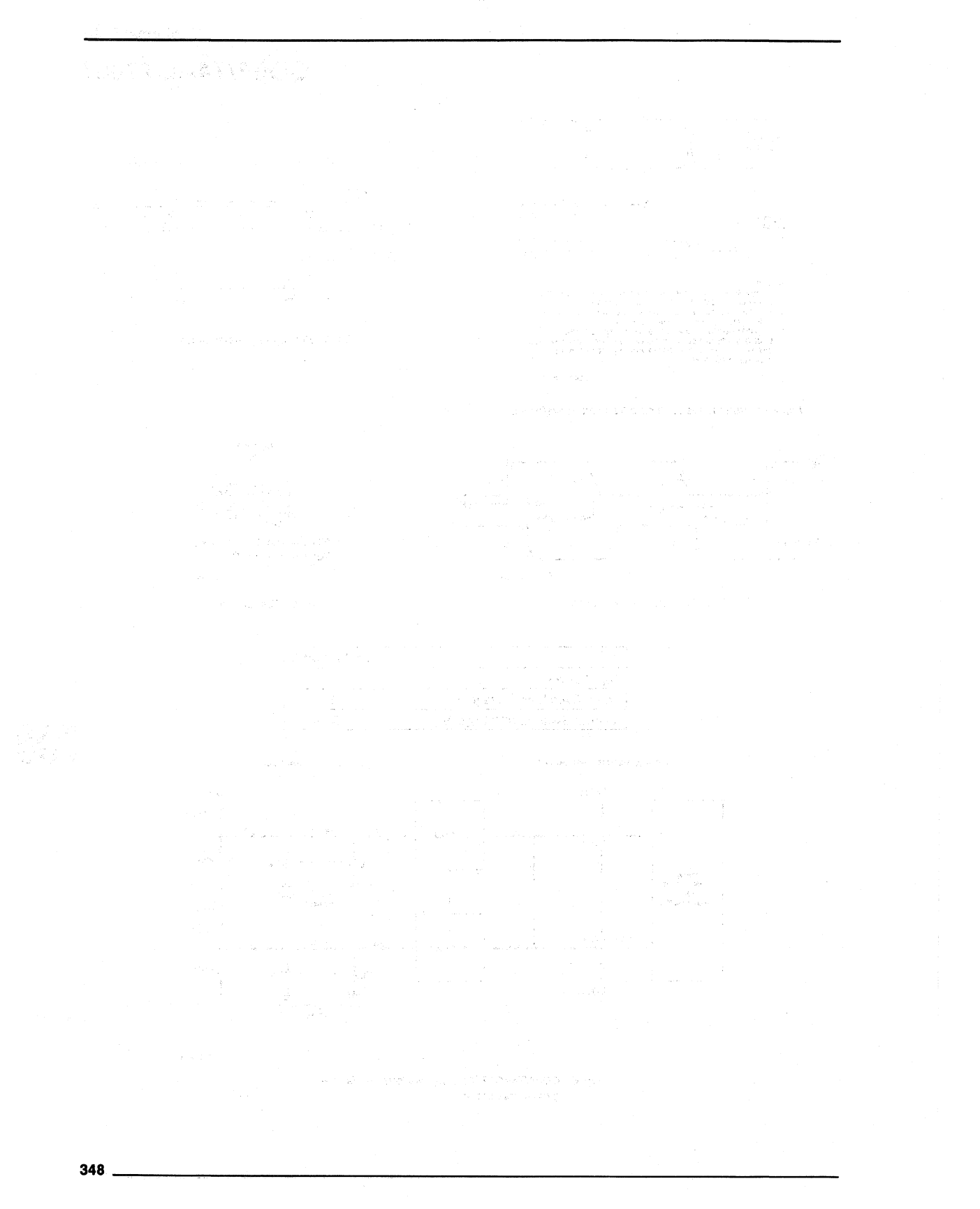


Fig. 6 - CD54/74ACT7651 computer/bus interface — typical application.



Military and Aerospace CD54AC/ACT Slash-Series ICs

Note: Refer to GE Solid State High-Reliability Products Data Book (SSD-230C, Volume I) for more detailed information.

RCA AC/ACT Slash Series

CMOS-Compatible Logic	TTL-Compatible Logic	Description	Pins
CERDIP	CERDIP		
CD54AC00F/3A	CD54ACT00F/3A	Quad 2-Input NAND Gate	14
CD54AC02F/3A	CD54ACT02F/3A	Quad 2-Input NOR Gate	14
CD54AC04F/3A	CD54ACT04F/3A	Hex Inverter/Buffer	14
CD54AC05F/3A	CD54ACT05F/3A	Hex Inverter/Buffer with Open-Drain Outputs	14
CD54AC08F/3A	CD54ACT08F/3A	Quad 2-Input AND Gate	14
CD54AC10F/3A	CD54ACT10F/3A	Triple 3-Input NAND Gate	14
*CD54AC14F/3A	*CD54ACT14F/3A	Hex Inverting Schmitt Trigger	14
CD54AC20F/3A	CD54ACT20F/3A	Dual 4-Input NAND Gate	14
CD54AC32F/3A	CD54ACT32F/3A	Quad 2-Input OR Gate	14
CD54AC74F/3A	CD54ACT74F/3A	Dual D Flip-Flop w/Set and Reset	14
CD54AC86F/3A	CD54ACT86F/3A	Quad 2-Input Exclusive-OR Gate	14
CD54AC109F/3A	CD54ACT109F/3A	Dual J-K Flip-Flop w/Set and Reset	16
CD54AC112F/3A	CD54ACT112F/3A	Dual J-K Flip-Flop w/Set and Reset	
CD54AC138F/3A	CD54ACT138F/3A	3-to-8-Line Decoder/Demultiplexer, Inverting	16
CD54AC139F/3A	CD54ACT139F/3A	Dual 2-to-4 Line Decoder/ Demultiplexer	16
CD54AC151F/3A	CD54ACT151F/3A	8-Input Multiplexer	16
CD54AC153F/3A	CD54ACT153F/3A	Dual 4-Input Multiplexer	16
CD54AC157F/3A	CD54ACT157F/3A	Quad 2-Input Multiplexer	16
CD54AC158F/3A	CD54ACT158F/3A	Quad 2-Input Multiplexer, Inverting	16
CD54AC161F/3A	CD54ACT161F/3A	Synchronous 4-Bit Binary Counter, Asynchronous Reset	16
CD54AC163F/3A	CD54ACT163F/3A	Synchronous 4-Bit Binary Counter, Synchronous Reset	16
CD54AC164F/3A	CD54ACT164F/3A	8-Bit Serial-In Parallel-Out Shift Register	14
CD54AC174F/3A	CD54ACT174F/3A	Hex D-Type Flip-Flop w/Reset	16
CD54AC175F/3A	CD54ACT175F/3A	Quad D-Type Flip-Flop w/Reset	16
CD54AC191F/3A	CD54ACT191F/3A	Synchronous 4-Bit Binary Up/Down Counter	16
CD54AC193F/3A	CD54ACT193F/3A	Synchronous 4-Bit Binary Up/Dow Counter	16
CD54AC238F/3A	CD54ACT238F/3A	3-to-8-Line Decoder/Demultiplexer	16
CD54AC240F/3A	CD54ACT240F/3A	Octal Buffer/Line Driver, 3-State, Inverting	20
CD54AC241F/3A	CD54ACT241F/3A	Octal-Buffer/Line Driver, 3-State	20
CD54AC244F/3A	CD54ACT244F/3A	Octal-Buffer/Line Driver, 3-State	20
CD54AC245F/3A	CD54ACT245F/3A	Octal-Bus Transceiver, 3-State	20
CD54AC251F/3A	CD54ACT251F/3A	8-Input Multiplexer, 3-State	16
CD54AC253F/3A	CD54ACT253F/3A	Dual 4-Input Multiplexer, 3-State	16
CD54AC257F/3A	CD54ACT257F/3A	Quad 2-Input Multiplexer, 3-State	16
CD54AC258F/3A	CD54ACT258F/3A	Quad 2-Input Multiplexer, 3-State	16
CD54AC273F/3A	CD54ACT273F/3A	Octal D-Type Flip-Flop w/Reset	20
CD54AC280F/3A	CD54ACT280F/3A	9-Bit Odd/Even Parity Generator/Checker	14
CD54AC283F/3A	CD54ACT283F/3A	4-Bit Full Adder w/Fast Carry	16
CD54AC299F/3A	CD54ACT299F/3A	8-Bit Universal Shift Register, 3-State	20
CD54AC323F/3A	CD54ACT323F/3A	8-Bit Universal Shift Register, 3-State (with Synchronous Reset)	20
CD54AC373F/3A	CD54ACT373F/3A	Octal Transparent Latch, 3-State	20
CD54AC374F/3A	CD54ACT374F/3A	Octal D Flip-Flop, 3-State	20
CD54AC533F/3A	CD54ACT533F/3A	Octal Transparent Latch, 3-State Inverting	20
CD54AC534F/3A	CD54ACT534F/3A	Octal D Flip-Flop, 3-State, Inverting	20

*Future availability is under consideration. Contact your local GE Solid State Sales Office for availability status.

RCA AC/ACT Slash Series (Cont'd)

CMOS-Compatible Logic	TTL-Compatible Logic	Description	Pins
CERDIP	CERDIP		
CD54AC540F/3A	CD54ACT540F/3A	Octal Buffer/Line Driver, 3-State Inverting	20
CD54AC541F/3A	CD54ACT541F/3A	Octal Buffer/Line Driver, 3-State	20
CD54AC563F/3A	CD54ACT563F/3A	Octal Inverting Transparent Latch, 3-State	20
CD54AC564F/3A	CD54ACT564F/3A	Octal D-Type Flip-Flop, 3-State Inverting	20
CD54AC573F/3A	CD54ACT573F/3A	Octal Transparent Latch, 3-State	20
CD54AC574F/3A	CD54ACT574F/3A	Octal D-Type Flip-Flop, 3-State	20
CD54AC623F/3A	CD54ACT623F/3A	Octal-Bus Transceiver, 3-State, Non-Inverting	20
*CD54AC646F/3A	*CD54ACT646F/3A	Octal Bus Transceiver/Register, 3-State	24
*CD54AC647F/3A	*CD54ACT647F/3A	Octal-Bus Transceiver/Register with Open Drain, Non-Inverting	24
*CD54AC648F/3A	*CD54ACT648F/3A	Octal Bus Transciever/Register, 3-State, Inverting	24
*CD54AC649F/3A	*CD54ACT649F/3A	Octal-Bus Transceiver/Register with Open Drain, Inverting	24
*CD54AC651F/3A	*CD54ACT651F/3A	Octal-Bus Tranceiver/Register, 3-State, Inverting	24
*CD54AC652F/3A	*CD54ACT652F/3A	Octal-Bus Transceiver/Register, 3-State, Non-Inverting	24
*CD54AC653F/3A	*CD54ACT653F/3A	Octal-Bus Transceiver/Register, Open-Drain (A Side); 3-State (B Side); Inverting	24
*CD54AC654F/3A	*CD54ACT654F/3A	Octal-Bus Transceiver/Register, Open-Drain (A Side); 3-State (B Side); Non-Inverting	24
*CD54AC7060F/3A	*CD54ACT7060F/3A	14-State Binary Counter with Oscillator	20
*CD54AC7201F/3A	*CD54ACT7201F/3A	512 x 9-Bit Parallel FIFO	28
*CD54AC7202F/3A	*CD54ACT7202F/3A	1024 x 9-Bit Parallel FIFO	28
CD54AC7623F/3A	CD54ACT7623F/3A	Octal-Bus Transceiver, 3-State (B Side), Open-Drain (A Side), Non-Inverting	20

*Future availability is under consideration. Contact your local GE Solid State Sales Office for availability status.

DESC Standard Military Drawing Cross-Reference Guide

BY STANDARD MILITARY DRAWING NUMBER

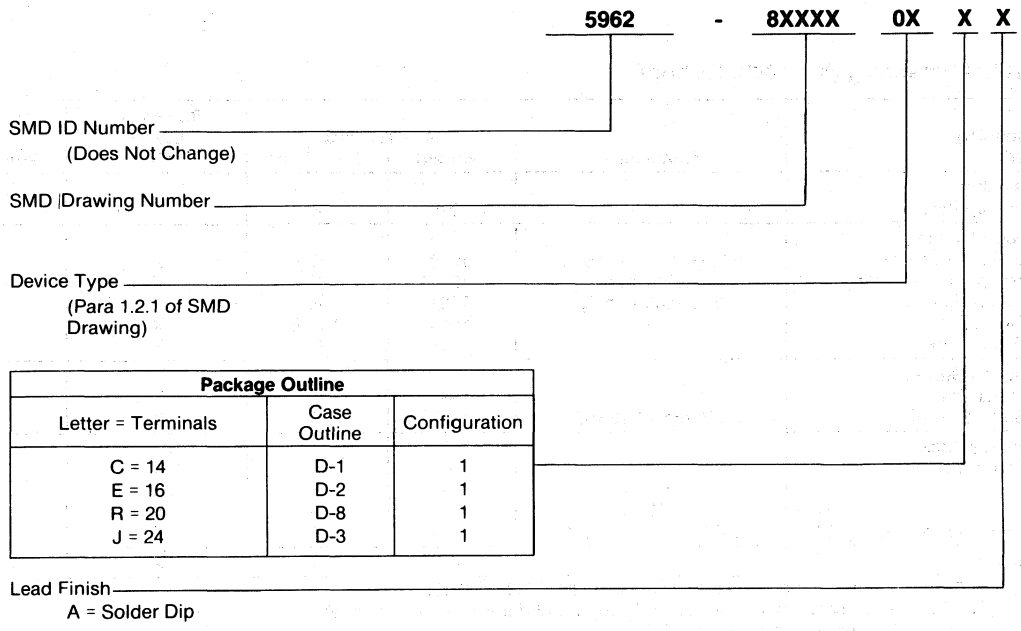
STANDARD MILITARY DRAWING #	RCA DEVICE
5962-8752501CA	CD54ACT74F3A
5962-8754901CA	CD54AC00F3A
5962-8755001RA	CD54AC240F3A
5962-8755101RA	CD54AC241F3A
5962-8755201RA	CD54AC244F3A
5962-8755301EA	CD54ACT139F3A
5962-8755401EA	CD54ACT138F3A
5962-8755501RA	CD54AC373F3A
5962-8755601RA	CD54ACT373F3A
5962-8760901CA	CD54AC04F3A
5962-8761001CA	CD54AC10F3A
5962-8761201CA	CD54AC02F3A
5962-8761301CA	CD54AC20F3A
5962-8761401CA	CD54AC32F3A
5962-8761501CA	CD54AC08F3A
5962-8762201EA	CD54AC138F3A
5962-8762301EA	CD54AC139F3A
5962-8762401CA	CD54AC14F3A
5962-8762501EA	CD54AC153F3A
5962-8762601EA	CD54AC174F3A
5962-8763101RA	CD54ACT374F3A
5962-8766301RA	CD54ACT245F3A
5962-8769101EA	CD54AC151F3A
5962-8769201EA	CD54AC251F3A
5962-8769301EA	CD54AC253F3A
5962-8769401RA	CD54AC374F3A
5962-8769501RA	CD54AC540F3A
5962-8769901CA	CD54ACT00F3A
5962-8775601RA	CD54AC273F3A
5962-8775701EA	CD54ACT174F3A
5962-8775801RA	CD54AC245F3A
5962-8775901RA	CD54ACT240F3A
5962-8776001RA	CD54ACT244F3A
5962-8776101EA	CD54ACT253F3A
5962-8852001CA	CD54AC74F3A
5962-8853401EA	CD54ACT109F3A

BY RCA DEVICE TYPE

RCA DEVICE	STANDARD MILITARY DRAWING #
CD54AC00F3A	5962-8754901CA
CD54ACT00F3A	5962-8769901CA
CD54AC02F3A	5962-8761201CA
CD54AC04F3A	5962-8760901CA
CD54AC08F3A	5962-8761501CA
CD54AC10F3A	5962-8761001CA
CD54AC14F3A	5962-8762401CA
CD54AC20F3A	5962-8761301CA
CD54AC32F3A	5962-8761401CA
CD54AC74F3A	5962-8852001CA
CD54ACT74F3A	5962-8752501CA
CD54ACT109F3A	5962-8853401EA
CD54AC138F3A	5962-8762201EA
CD54ACT138F3A	5962-8755401EA
CD54AC139F3A	5962-8762301EA
CD54ACT139F3A	5962-8755301EA
CD54AC151F3A	5962-8769101EA
CD54AC153F3A	5962-8762501EA
CD54AC174F3A	5962-8762601EA
CD54ACT174F3A	5962-8775701EA
CD54AC240F3A	5962-8755001RA
CD554ACT240F3A	5962-8775901RA
CD54AC241F3A	5962-8755101RA
CD54AC244F3A	5962-8755201RA
CD54ACT244F3A	5962-8776001RA
CD54AC245F3A	5962-8775801RA
CD54ACT245F3A	5982-8766301RA
CD54AC251F3A	5982-8769201EA
CD54AC253F3A	5962-8769301EA
CD54ACT253F3A	5962-8776101EA
CD54AC273F3A	5962-8775601RA
CD54AC373F3A	5962-8755501RA
CD54ACT373F3A	5962-8755601RA
CD54AC374F3A	5962-8769401RA
CD54ACT374F3A	5962-8763101RA
CD54AC540F3A	5962-8769501RA

Contact your local GE Solid State Sales Office for availability status.

DESC Standard Military Drawing Nomenclature Guide



Package Outline		
Letter = Terminals	Case Outline	Configuration
C = 14	D-1	1
E = 16	D-2	1
R = 20	D-8	1
J = 24	D-3	1

Screening and Conformance Testing

Lot Screening Tests

/3A Screening Level is Compliant to MIL-STD-883, Para. 1.2.1

Total Lot Screening (X = 100% Testing)

Screening Tests	Conditions	MIL-STD-883 Method	MIL-STD-883 Conditions	Screening Levels /3A	Notes
Assembly					
Precap Visual		2010	B	X	
Preconditioning					
Stabilization Bake	24 hrs. min. at 150°C	1008	C	X	
Temperature Cycling	10 Cycles	1010	C	X	
Centrifuge	Y_1 direction only	2001	E	X	
Fine Leak	—	1014	A or B	X	
Gross Leak	—	1014	C	X	
Test and Burn-in					
Initial Test	—	—	—	X	
Static Burn-in	120 hrs. @ 135°C	1015	B	X	1
Final Electrical					
Static Electrical (DC)	25°C	—	—	X	2, 3
	-55°C	—	—	X	
	+125°C	—	—	X	
Dynamic Electrical (AC)	25°C, -55°C, +125°C	—	—	X	
Group A	—	—	X	X	4

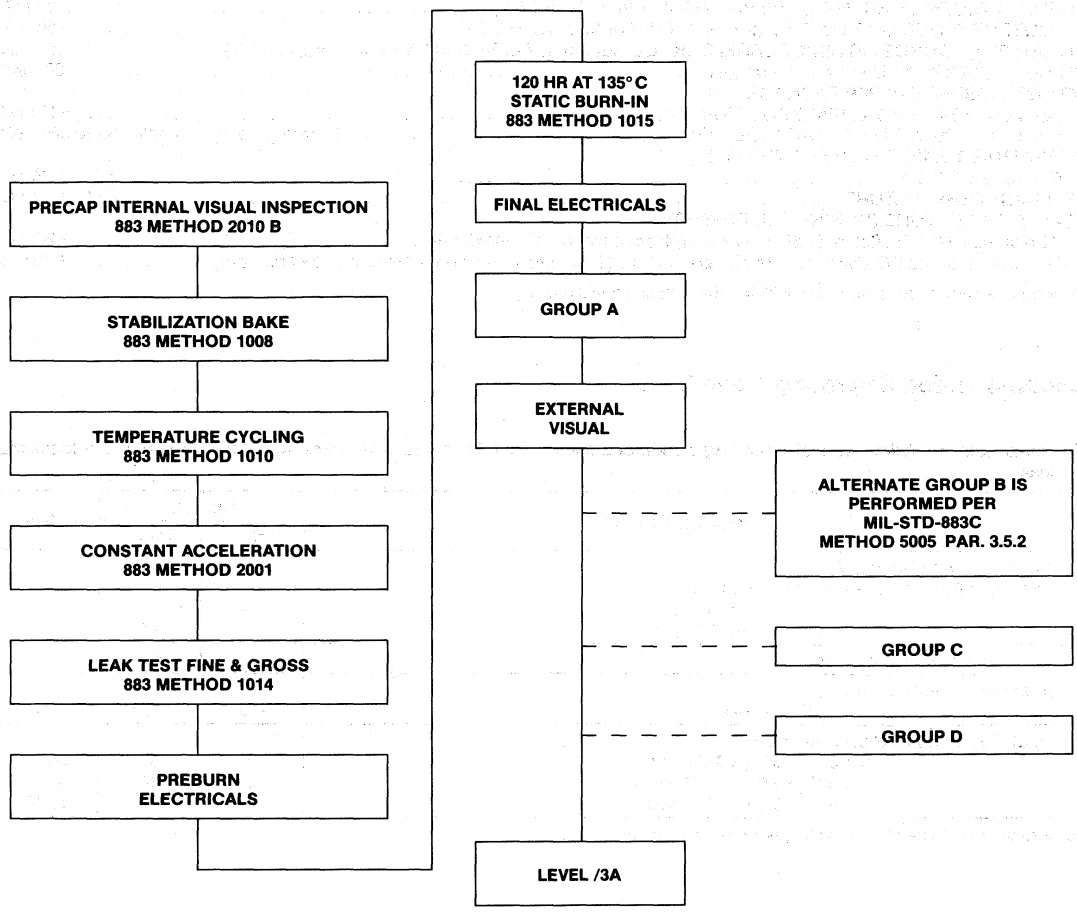
Notes: 1. Alternate time/temperature regression used per Method 1015.
2. All electrical testing per parameters shown in individual device data sheets.
3. PDA = 5%, one reburn allowed at 3%.
4. Sample test performed per Method 5005 of MIL-STD-883.

Manufacturing and Conformance Testing

Characteristic	/3A[1]
SERIES	AC, ACT
PACKAGE	F
DIE ATTACH	EUTECTIC
LEAD FINISH	SOLDER DIP
MANUFACTURING LOCATION	OFF-SHORE
SCREENING	METHOD 5004
CONFORMANCE TESTS	
GROUP A	METHOD 5005
CLASS B, GROUP B[2]	METHOD 5005
CLASS B, GROUP C	METHOD 5005
GROUP D	METHOD 5005
DATA SUPPLIED	
C OF C[3]	YES

NOTES:
1. Slash 3A meets MIL-STD-883 Class B (compliant to Para. 1.2.1).
2. For Slash 3A Series, Group B will conform to MIL-STD-883 using the alternate Group B Method 5005 (Para. 3.5.2).
3. Certificate of compliance (C of C) signed by RCA representative provides identity and customer order number, and lists and certifies tests, methods and conditions per MIL-STD-883. Group A and B attributes data will be supplied.

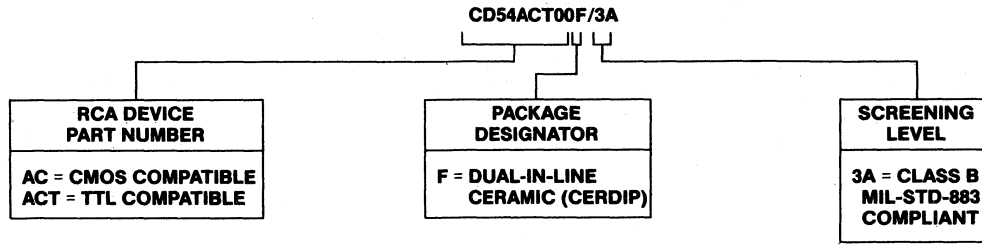
Product Flow Diagram



RCA HIGH-RELIABILITY LEVEL /3A 54AC/ACT ICs
(Screened to Method 5004 of MIL-STD-883C)

10

Guide to the Reliability Class and Package of RCA High-Reliability 54AC/ACT Integrated Circuits



Ratings and Characteristics

Maximum Ratings, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to +6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) ..... ±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) ..... ±50 mA
DC V_{CC} or GROUND CURRENT (I_{CC} or I_{GND}) ..... ±100 mA*
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE F) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/°C to 300 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

*(For up to 4 outputs per device, add ± 25 mA for each additional output.)

Recommended Operating Conditions:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}* (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	
Operating Temperature, T_A:			
CD54 Types	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (AC Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

FCT Bus-Interface Family—
TTL Backplane-Interface Logic Family in Advanced CMOS Technology

11

FCT PRODUCTS FOR BACKPLANE-INTERFACE APPLICATIONS

RCA FCT products are being developed to provide a reliable interface with modern high-speed backplanes. The FCT types vastly reduce power consumption, avoid bus contention difficulties, minimize switching noise, and provide outputs that are specifically tailored to interface with VME buses or their equivalent.

The speed of the FCT family is comparable to that of bipolar FAST types. Sink current ranges from 48 milliamperes to 64 milliamperes depending on product type. Fully populated buses, such as the 21-slot VME can be reliably interfaced. Products are most economically packaged in plastic DIP and gull-wing surface-mount pinouts. As with GE's AC/ACT family of logic devices, simultaneous switching transients are controlled to levels comparable to similar bipolar logic functions (1 volt peak area for octal ground bounce).

FCT products, the modern standard for backplane-interface applications, meet or exceed planned JEDEC industry-standard No. 18 specifications. FCT products clearly are the low-power backplane interface needed in the rapidly growing down-sized computer world, where low operating power and virtually zero standby power are essential requirements.

The two competitive bipolar families, FAST and the proposed BCT line as described in the technical press, compared with FCT products are 300 to 1000 times higher in quiescent power consumption and 400 to 850 times higher in operating power consumption at a continuous five megahertz operation. This comparison is illustrated in Fig. 79.

The ratio of sink-to-source current and the absence of diodes clamped to the supply rail at the I/O ports eliminate or minimize bus contention and permit low power-down mode operation.

Table XVIII lists types and type numbers now in planning.

FCT Features

Speed	Competitive with similar bipolar F/AS TTL functions. Typical delay is 3.5 nanoseconds.
Sink/Source Current	All types have sink and source currents meeting VME, multibus, etc standards. Output edges are monotonic through the TTL switch point with fully populated backplanes.
Simultaneous Switching Transients	(Ground bounce) Competitive with similar bipolar TTL and CMOS products. Output swing is 3.5 volts. Output edges are slewed.
Operating and Standby Power	Ultra-low pure CMOS operating power and standby power of almost zero.
Pinout	Standard.

FCT Benefits

Swift delay requirements dictated by modern control-system backplane-interface logic present no problems.

Optimized output drives minimize backplane reflections in worst-case situations.

EMI and RFI emissions minimized. Good signal-pulse integrity.

Meets low-power needs of down-sized computers without fans, etc. Low battery drain.

Provided in minimum and most economically sized DIP and SOP.

Minimum CAD/CAM, burn-in board, and PC-board real-estate costs. With no performance sacrifice.

Table XVIII - Planned FCT Types

Buffers			
CD54/74FCT240	CD54/74FCT241	CD54/74FCT244	CD54/74FCT540
CD54/74FCT541	CD54/74FCT827	CD54/74FCT828	
Transceivers			
CD54/74FCT245	CD54/74FCT623	CD54/74FCT646	CD54/74FCT648
CD54/74FCT651	CD54/74FCT652	CD54/74FCT861	CD54/74FCT862
CD54/74FCT863	CD54/74FCT864	CD54/74FCT7623	
Latches			
CD54/74FCT373	CD54/74FCT533	CD54/74FCT563	CD54/74FCT573
CD54/74FCT841	CD54/74FCT842	CD54/74FCT843	CD54/74FCT844
Registers			
CD54/74FCT821	CD54/74FCT822	CD54/74FCT823	CD54/74FCT824
Flip-Flops			
CD54/74FCT273	CD54/74FCT374	CD54/74FCT534	CD54/74FCT564
CD54/74FCT574			

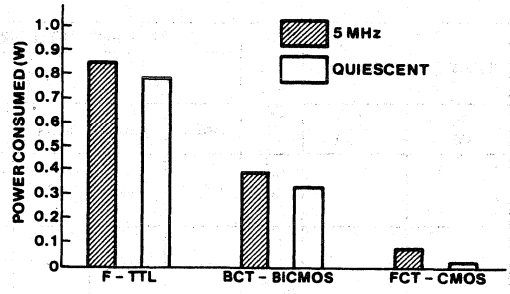


Fig. 79 - Comparison of power consumption for an octal transceiver type.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{CC}) ..... -0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ V) ..... -20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ V) ..... -50 mA
DC OUTPUT SINK CURRENT per Output Pin, I_O ..... +70 mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O ..... -30 mA
DC V_{CC} CURRENT (I_{CC}) ..... 140 mA
DC GROUND CURRENT (I_{GND}) ..... N (I_{OL}) + M (ΔI_{CC})
where N = No. of outputs
M = No. of inputs

POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE E, M ..... -55 to +125°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC}*:			
T_A = 0 to 70°C	4.75	5.25	V
T_A = -55 to + 125°C	4.5	5.5	
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS

FCT Series:

74FCT Commercial Temperature Range, 0 to 70°C. V_{CC} max = 5.25 V, V_{CC} min = 4.75 V

54FCT Extended Industrial Temperature Range, -55 to +125°C. V_{CC} max = 5.5 V, V_{CC} min = 4.5 V

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
					+25		0 to +70		-55 to +125		
		V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2	—	2	—	2	—	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15#	MIN.	2.4	—	2.4	—	—	—	V
			-12#		2.4	—	—	—	2.4	—	
Low-Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64#	MIN.	—	0.55	—	0.55	—	—	
			48#		—	0.55	—	—	—	0.55	
High-Level Input Current	I_{IH}	V_{CC}		MAX.	—	0.1	—	1	—	1	μA
Low-Level Input Current	I_{IL}	GND		MAX.	—	-0.1	—	-1	—	-1	μA
3-State Leakage Current	I_{OZH}	V_{CC}		MAX.	—	0.5	—	10	—	10	μA
	I_{OZL}	GND		MAX.	—	-0.5	—	-10	—	-10	
Short-Circuit Output Current*	I_{OS}	V_{CC} or GND V_O = 0		MAX.	-60#	—	-60#	—	-60#	—	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	MIN.	—	-1.2	—	-1.2	—	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	MAX.	—	8	—	80	—	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI_{CC}	3.4 V†		MAX.	—	1.6	—	1.6	—	2	mA

*Not more than one output should be shorted at one time. Test duration should not exceed 100 ms.

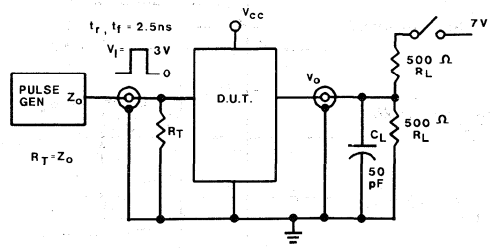
†Inputs that are not measured are at V_{CC} or Gnd.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6 mA max. @ 70°C.

#Values are for FCT240 types (see "Output Capabilities" and Table XIX for I_{OS}, I_{OL}, and I_{OH} for other types.)

SWITCHING WAVEFORMS FOR 54/74FCTXXX

Shown below is the FCT test circuit. A Thevenin equivalent may be used for output loading.



TEST	SWITCH POSITION
t_{PLZ} t_{PZL} OPEN DRAIN	CLOSED
t_{PHZ} t_{PZH} t_{PLH} t_{PHL}	OPEN

Definitions:

C_L = Load capacitance includes jig and probe capacitance.
R_T = Termination should be equal to Z_{OUT} of the pulse generator. (Typically 50 Ω).
V_{IN} = 0 V to 3 V
Input: $t_r = t_f$ = 2.5 ns (10% to 90%) unless otherwise specified.

Fig. 80 - Test circuit.

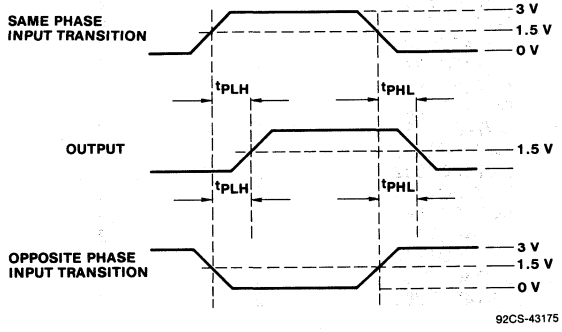
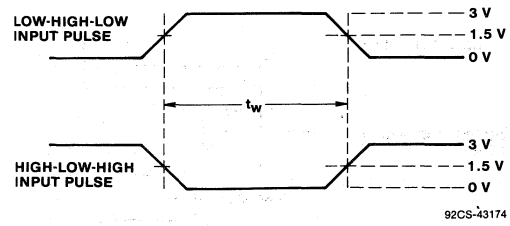


Fig. 81 - Propagation delay times.



Output Requirement:

Device must follow truth table.
$V_{OL} \leq 0.55$ V
$V_{OH} \geq 2.4$ V

Input Condition:

$t_r = t_f \leq 2.5$ ns (as fast as required)

Standard Output Loading:

R_L = 500 Ω
C_L = 50 pF

Fig. 82 - Input pulse width.

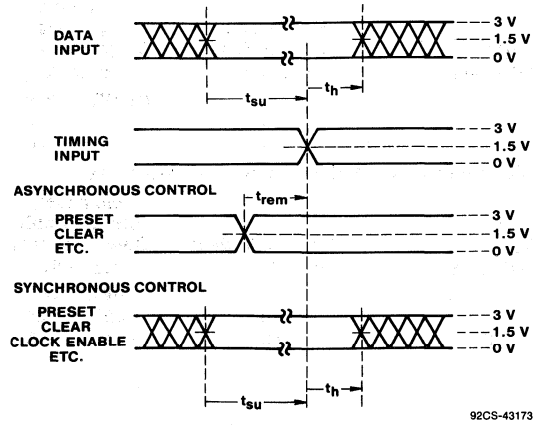


Fig. 83 - Setup, hold, and removal times.

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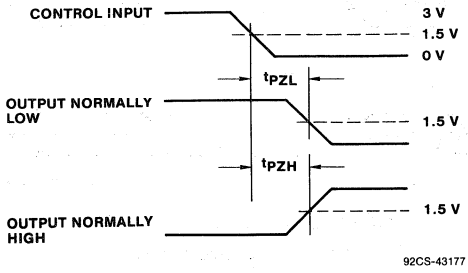
SWITCHING WAVEFORMS FOR 54/74FCTXXX (CONT'D)

ENABLE TIMES



DISABLE TIMES

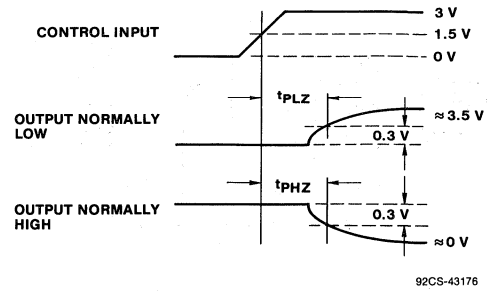


Fig. 84 - Output enable and disable times.

OUTPUT CAPABILITIES

Because of the numerous applications for 54/74FCT types, the output specifications are derived from the LOW drive and HIGH drive tables below. Any I_{OL} type category may be combined with any I_{OH} and I_{OS} type category to specify the output drive. Refer to Table XIX for device type categories.

Minimum Output at Low Drive (I_{OL}); V_{CC} = min

Type Category	Low-Level Output Voltage V_{OL} (V)	Minimum Low-Level Output Current I_{OL} (mA)	
		COM'L	MIL
3	0.55	48	32
4	0.55	64	48

Minimum Output at High Drive (I_{OH}); V_{CC} = min

Type Category	High-Level Output Voltage V_{OH} (V)	Minimum High-Level Output Current I_{OH} (mA)	
		COM'L	MIL
1	2.4	-15	-12
2	2.4	-24	-20

Minimum Output at Short Circuit (I_{OS}); V_{CC} = max

Type Category	Output Voltage V_O (V)	Minimum Short-Circuit Output Current I_{OS} (mA)	
		COM'L	MIL
1	0.0	-60	-60
2	0.0	-75	-75

Table XIX - Output Drive for 54/74FCTXXX

Device Number	I_{OH} Output Type	I_{OL} Output Type
54/74FCT240	1	4
54/74FCT241	1	4
54/74FCT244	1	4
54/74FCT245	1	4
54/74FCT273	1	3
54/74FCT373	1	3
54/74FCT374	1	3
54/74FCT533	1	3
54/74FCT534	1	3
54/74FCT540	1	4
54/74FCT541	1	4
54/74FCT563	1	3
54/74FCT564	1	3
54/74FCT573	1	3
54/74FCT574	1	3
54/74FCT623/7623	1	4
54/74FCT646	1	4
54/74FCT648	1	4
54/74FCT651	1	4
54/74FCT652	1	4
54/74FCT821	2	3
54/74FCT822	2	3
54/74FCT823	2	3
54/74FCT824	2	3
54/74FCT827	2	3
54/74FCT828	2	3
54/74FCT842	2	3
54/74FCT843	2	3
54/74FCT844	2	3
54/74FCT861	2	3
54/74FCT862	2	3
54/74FCT863	2	3
54/74FCT864	2	3

PRELIMINARY SWITCHING-SPEED LIMITS

This section gives the preliminary switching-speed parameter limits for the FCT types. The limits are given for each type grouped by generic function. Table XX covers bus drivers, buffers, and transceivers. Table XXI covers flip-flops and registers. Table XXII covers latches, and Table XXIII covers all types that additionally have three-state operation capability.

In the tables, individual parameter limits are given for each device type along with descriptive symbols for each parameter. All limit values are in nanoseconds. Generic pin names are used and no distinctions are made for inverting or non-inverting outputs unless noted.

For each entry two limit values are shown separated by a slash, e.g. a/b. Limit a applies to the commercial temperature range 0 to 70° C with V_{CC} = 5.0 ± 0.25 volts. Limit b applies to the MIL temperature range of -55° C to +125° C with V_{CC} = 5.0 ± 0.5 volts. Plastic DIP and SOP packaged parts (74 series) are applicable for both temperature ranges. The 54 series devices will apply only to the MIL ceramic packaged parts when available. A dash (—) indicates that the parameter is not specified or does not exist for a given device.

It should be noted that these preliminary speed limits are design objectives and are subject to possible minor changes.

Table XX - Switching Parameters for Bus Drivers, Buffers, and Transceivers.

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT240	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	8.0/9.0
CD54/74FCT241	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	6.5/7.0
CD54/74FCT244	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	6.5/7.0
CD54/74FCT245	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	7.0/7.5
CD54/74FCT540	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	8.0/9.0
CD54/74FCT541	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	6.5/7.0
CD54/74FCT623	t_{PLH}, t_{PHL} $A_n/B_n \rightarrow Y_n$	7.0/7.5
	t_{PZH}, t_{PZL} $G, \overline{G} \rightarrow O$	9.5/10.0
	t_{PHZ}, t_{PLZ} $G, \overline{G} \rightarrow O$	7.5/10.0
CD54/74FCT646	t_{PLH}, t_{PHL} BUS→Bus	9.0/11.0
	t_{PLH}, t_{PHL} CL→Bus	9.0/10.0
	t_{PLH}, t_{PHL} Sel→Bus	11.0/12.0
	t_{PZH}, t_{PZL} $\overline{G}$/DIR→Bus	14.0/15.0
	t_{PHZ}, t_{PLZ} $\overline{G}$/DIR→Bus	9.0/11.0
	t_{su}	4.0/4.5
	t_h	2.0/2.0
	t_{pw}	6.0/6.0
CD54/74FCT648	t_{PLH}, t_{PHL} BUS→Bus	8.0/9.0
	t_{PLH}, t_{PHL} CL→Bus	9.0/10.0
	t_{PLH}, t_{PHL} Sel→Bus	11.0/12.0
CD54/74FCT648 (cont'd)	t_{PZH}, t_{PZL} $\overline{G}$/DIR→Bus	15.0/18.0
	t_{PHZ}, t_{PLZ} $\overline{G}$/DIR→Bus	9.0/11.0
	t_{su}	4.0/4.5
	t_h	2.0/2.0
	t_{pw}	6.0/6.0
CD54/74FCT651	t_{PLH}, t_{PHL} BUS→Bus	9.0/10.0
	t_{PLH}, t_{PHL} CL→Bus	9.0/11.0
	t_{PLH}, t_{PHL} Sel→Bus	11.0/12.0
	t_{PZH}, t_{PZL} $\overline{G}$/DIR→Bus	14.0/13.0
	t_{PHZ}, t_{PLZ} $\overline{G}$/DIR→Bus	9.0/11.0
	t_{su}	4.0/4.5
	t_h	2.0/2.0
	t_{pw}	6.0/6.0
CD54/74FCT652	t_{PLH}, t_{PHL} BUS→Bus	9.0/10.0
	t_{PLH}, t_{PHL} CL→Bus	9.0/11.0
	t_{PLH}, t_{PHL} Sel→Bus	11.0/12.0
	t_{PZH}, t_{PZL} $\overline{G}$/DIR→Bus	14.0/13.0
	t_{PHZ}, t_{PLZ} $\overline{G}$/DIR→Bus	9.0/11.0
	t_{su}	4.0/4.5
	t_h	2.0/2.0
	t_{pw}	6.0/6.0
CD54/74FCT827	t_{PLH}, t_{PHL} $A_n \rightarrow Y_n$	10.0/12.0

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Table XX - Switching Parameters for Bus Drivers, Buffers, and Transceivers (Cont'd)

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT827 (cont'd)	t_{PLZ},t_{PHZ} G→O	13.0/15.0
	t_{PZL},t_{PZH} G→O	13.0/15.0
CD54/74FCT828	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	13.0/15.0
	t_{PZL},t_{PZH} G→O	13.0/15.0
CD54/74FCT861	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	14.0/16.0
	t_{PZL},t_{PZH} G→O	14.0/16.0
CD54/74FCT862	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	14.0/16.0

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT862 (cont'd)	t_{PZL},t_{PZH} G→O	14.0/16.0
CD54/74FCT863	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	14.0/16.0
	t_{PZL},t_{PZH} G→O	14.0/16.0
CD54/74FCT864	t_{PLH},t_{PHL} A_n→Y_n	10.0/12.0
	t_{PLZ},t_{PHZ} G→O	14.0/16.0
	t_{PZL},t_{PZH} G→O	14.0/16.0
CD54/74FCT7623	t_{PLH},t_{PHL} A_n→Y_n	7.0/7.5
	t_{PLZ} B_n→Y_n	7.5/10.0
	t_{PZL} B_n→Y_n	9.5/10.0

Table XXI - Switching Parameters for Flip-Flops and Registers

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT273	t_{PLH},t_{PHL} CK→Q	13.0/15.0
	t_{PLH},t_{PHL} R,S→Q	13.0/15.0
	t_{su} D,J,K→CK	3.0/3.5
	t_h CK→D,J,K	2.5/2.5
	t_{rem} R,S→CK	4.0/5.0
	t_w(CK)	7.0/7.0
	t_w(R,S)	7.0/7.0
CD54/74FCT374	t_{PLH},t_{PHL} CK→Q	10.0/11.0
	t_{su} D,J,K→CK	2.0/2.5
	t_h CK→D,J,K	2.0/2.5
	t_w(CK)	7.0/7.0
CD54/74FCT534	t_{PLH},t_{PHL} CK→Q	10.0/11.0
	t_{su} D,J,K→CK	2.0/2.5

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT534 (cont'd)	t_h CK→D,J,K	2.0/2.5
	t_w(CK)	7.0/7.5
	t_{su} CE→CK	—
	t_h CE→CK	—
CD54/74FCT564	t_{PLH},t_{PHL} CK→Q	10.0/11.0
	t_{su} D,J,K→CK	2.0/2.5
	t_h CK→D,J,K	2.0/2.5
	t_w(CK)	7.0/7.5
	t_{su} CE→CK	—
	t_h CE→CK	—
CD54/74FCT574	t_{PLH},t_{PHL} CK→Q,Q	10.0/11.0
	t_{su} D,J,K→CK	2.0/2.5
	t_h CK→D,J,K	2.0/2.5

Table XXI - Switching Parameters for Flip-Flops and Registers (Cont'd)

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT574 (cont'd)	t_w(CK)	7.0/7.0
	t_{PLZ},t_{PHZ} G→O	8.0/8.0
	t_{PZL},t_{PZH} G→O	12.5/14.0
CD54/74FCT821	t_{PLH},t_{PHL} CK→Q,Q	12.0/14.0
	t_{su} D,J,K→CK	4.0/6.0
	t_h CK→D,J,K	2.0/3.0
	t_w(CK)	7.0/11.0
	t_{PLZ},t_{PHZ} G→O	12.0/14.0
	t_{PZL},t_{PZH} G→O	12.0/14.0
CD54/74FCT822	t_{PLH},t_{PHL} CK→Q,Q	12.0/14.0
	t_{su} D,J,K→CK	4.0/6.0
	t_h CK→D,J,K	2.0/3.0
	t_w(CK)	7.0/11.0
	t_{PLZ},t_{PHZ} G→O	12.0/12.0
	t_{PZL},t_{PZH} G→O	12.0/14.0
CD54/74FCT823	t_{PLH},t_{PHL} CK→Q,Q	12.0/14.0
	t_{PLH},t_{PHL} R,S→Q,Q	13.0/15.0
	t_{su} D,J,K→CK	4.0/6.0

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT823 (cont'd)	t_h CK→D,J,K	2.0/3.0
	t_{rem} R,S→CK	7.0/7.0
	t_w(CK)	7.0/11.0
	t_w(R,S)	7.0/11.0
	t_{su} CE→CK	4.0/6.0
	t_h CE→CK	2.0/3.0
	t_{PLZ},t_{PHZ} G→O	12.0/12.0
	t_{PZL},t_{PZH} G→O	12.0/14.0
CD54/74FCT824	t_{PLH},t_{PHL} CK→Q,Q	12.0/14.0
	t_{PLH},t_{PHL} R,S→Q,Q	13.0/15.0
	t_{su} D,J,K→CK	4.0/6.0
	t_h CK→D,J,K	2.0/3.0
	t_{rem} R,S→CK	7.0/7.0
	t_w(CK)	7.0/11.0
	t_w(R,S)	7.0/11.0
	t_{su} CE→CK	4.0/6.0
	t_h CE→CK	2.0/3.0
	t_{PLZ},t_{PHZ} G→O	12.0/12.0
	t_{PZL},t_{PZH} G→O	12.0/14.0

Table XXII - Switching Parameters for Latches

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT373	t_{PLH},t_{PHL} D→Q	8.0/8.5
	t_{PLH},t_{PHL} E→Q	13.0/15.0
	t_{su} D→E	2.0/2.0
	t_h E→D	3.0/3.0
	t_w (E)	6.0/6.0

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT533	t_{PLH},t_{PHL} D→Q	8.0/8.5
	t_{PLH},t_{PHL} E→Q	13.0/14.0
	t_{su} D→E	2.0/2.0
	t_h E→D	3.0/3.0
	t_w (E)	6.0/6.0

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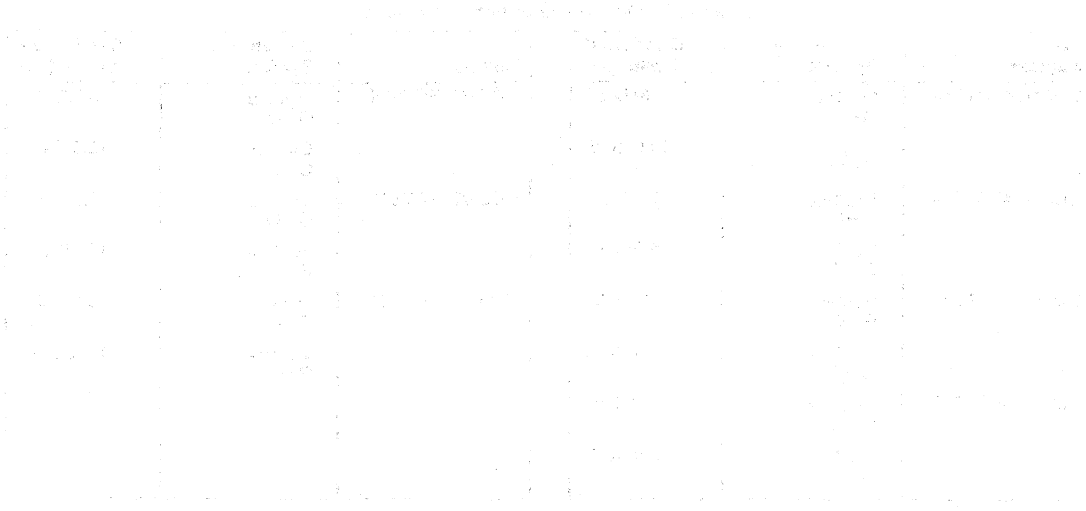
Table XXII - Switching Parameters for Latches (Cont'd)

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT563	t_{PLH},t_{PHL} D→Q	8.0/8.5
	t_{PLH},t_{PHL} E→Q	13.0/14.0
	t_{su} D→E	2.0/2.0
	t_h E→D	3.0/3.0
	t_w (E)	6.0/6.0
CD54/74FCT573	t_{PLH},t_{PHL} D→Q	8.0/8.5
	t_{PLH},t_{PHL} E→Q	13.0/15.0
	t_{su} D→E	2.0/2.0
	t_h E→D	3.0/3.0
	t_w (E)	6.0/6.0
	t_{PLZ},t_{PHZ} G→O	7.5/10.0
	t_{PZL},t_{PZH} G→O	12.0/13.5
CD54/74FCT841	t_{PLH},t_{PHL} D→Q	11.0/14.0
	t_{PLH},t_{PHL} E→Q	12.0/14.0
	t_{su} D→E	3.0/3.0
	t_h E→D	4.0/4.0
	t_w (E)	6.0/9.0
	t_{PLZ},t_{PHZ} G→O	12.0/14.0
	t_{PZL},t_{PZH} G→O	12.0/14.0
CD54/74FCT842	t_{PLH},t_{PHL} D→Q	11.0/14.0
	t_{PLH},t_{PHL} E→Q	12.0/14.0
	t_{su} D→E	3.0/3.0
	t_h E→D	4.0/4.0
	t_w (E)	6.0/9.0
CD54/74FCT842 (cont'd)	t_{PLZ},t_{PHZ} G→O	12.0/14.0
	t_{PZL},t_{PZH} G→O	12.0/14.0
CD54/74FCT843	t_{PLH},t_{PHL} D→Q	11.0/14.0
	t_{PLH},t_{PHL} E→Q	12.0/14.0
	t_{su} D→E	3.0/3.0
	t_h E→D	4.0/4.0
	t_w	6.0/9.0
	t_{PLH},t_{PHL} R,S→Q	13.0/15.0
	t_{su} S→E	4.0/4.0
	t_{su} R→E	3.0/3.0
	t_w R,S	8.0/12.0
	t_{PLZ},t_{PHZ} G→O	12.0/14.0
	t_{PZL},t_{PZH} G→O	12.0/14.0
CD54/74FCT844	t_{PLH},t_{PHL} D→Q	11.0/14.0
	t_{PLH},t_{PHL} E→Q	12.0/14.0
	t_{su} D→E	3.0/3.0
	t_h E→D	4.0/4.0
	t_w	6.0/9.0
	t_{PLH},t_{PHL} R,S→Q	13.0/15.0
	t_{su} S→E	4.0/4.0
	t_{su} R→E	3.0/3.0
	t_w R,S	8.0/12.0
	t_{PLZ},t_{PHZ} G→O	12.0/14.0
	t_{PZL},t_{PZH} G→O	12.0/14.0

Table XXIII - Three-State Switching Parameters

Type Number	Descriptive Symbol	COM'L/MIL Limits (ns)
CD54/74FCT240	t_{PLZ}, t_{PHZ} G→O	9.5/12.5
	t_{PZL}, t_{PZH} G→O	10.0/10.5
CD54/74FCT244	t_{PLZ}, t_{PHZ} G→O	7.0/7.5
	t_{PZL}, t_{PZH} G→O	8.0/8.5
CD54/74FCT245	t_{PLZ}, t_{PHZ} G→O	7.5/10.0
	t_{PZL}, t_{PZH} G→O	9.5/10.0
CD54/74FCT373	t_{PLZ}, t_{PHZ} G→O	7.5/10.0
	t_{PZL}, t_{PZH} G→O	12.0/13.5
CD54/74FCT374	t_{PLZ}, t_{PHZ} G→O	8.0/8.0
	t_{PZL}, t_{PZH} G→O	12.5/14.0
CD54/74FCT533	t_{PLZ}, t_{PHZ} G→O	7.0/8.5
	t_{PZL}, t_{PZH} G→O	11.0/12.5
CD54/74FCT534	t_{PLZ}, t_{PHZ} G→O	8.0/8.0
	t_{PZL}, t_{PZH} G→O	12.5/14.0



Application Notes

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ICAN-8640

Using Advanced CMOS Logic in a VME Data Bus System

J. Nadolski and Alan Kalish

SUMMARY

Advanced CMOS Logic (ACL) and High-Speed CMOS (74 types) are ideal for use in VME or any other system. Their benefits of low power consumption, high speed, excellent noise immunity, and wider operating-temperature range are important in system designs. This Note describes the performance of RCA's Advanced CMOS Logic and High-Speed CMOS in a VME system computer. The performance of the system with CMOS is compared to the unmodified off-the-shelf bipolar computer. ACL and High-Speed CMOS logic show greater tolerance to induced noise, and lower power consumption, than their bipolar equivalents. Data demonstrates that a system conversion to CMOS saved 9 watts of a total of 28 watts dissipated by the bipolar system without affecting system timing or operation.

INTRODUCTION

One of the biggest problems in any system is power and heat dissipation. These factors commonly cause the typical system to be larger and more expensive than the designer wishes. But now, with the advent of High-Speed CMOS and Advanced CMOS Logic, the system designer has an alternative to power-hungry bipolar glue logic.

This Note describes the benefits of using Advanced CMOS Logic from RCA in a VME system computer. The VME system was chosen over all others (e.g., multibus, standard bus, and S-100 bus) as an excellent candidate because of the large amount of glue logic used in it, and because this type of system would benefit most from the replacement of its bipolar glue parts, largely FAST and LSTTL. Advanced CMOS Logic has a drive capability of ±24 mA at 0.5V. The VME specification requires that drive logic be capable of driving 64 mA over a number of backplanes. Because of the lower drive current of the ACL logic, the number of backplanes is limited in this experiment to one VME and one VMX backplane, which have terminations of 330 and 470 ohms at each end. This limitation, imposed by drive current, should not prevent the user from reaping the benefits of replacing his bipolar logic with Advanced CMOS Logic, because in many systems only a few parts of many need adhere to the drive-logic specification. As highlighted in this paper, the advantages of using ACL are: much lower standby power, better reliability due to lower junction temperature and, because of the power savings, lower cost.

The data for this Note was collected first on the unmodified system, which contains bipolar bus interface logic (FAST and LSTTL). The system was tested in several operating modes. The 5-volt power supply was monitored with a clamp-on current probe, and waveform integrity was recorded. The system consists of a double-height 19-inch VME rack with power supply, both VME and VMX PCB buses, a system CPU controller with its internal memory, and two external I/O cards. Table I contains more detailed information on the system components.

The configuration of the system places the three cards evenly through the rack. The CPU card is at one end, the 6-port card is at the other, and the external CMOS RAM card is spaced evenly in the middle. Fig. 1 illustrates the configuration of the system in a block diagram.

Table I - System Components

Manufacturer	Model No.	Function
Force Computer	CPU-20	68020 CPU with 512K Memory
Force Computer	SRAM-1	128K CMOS RAM Card
Force Computer	SIO-1	6 I/O Serial Port
Force Computer	MOTH-12A	VME PCB Bus
Force Computer	MOTH-12E	VMX PCB Bus
Force Computer	PWR-09A	Power Supply

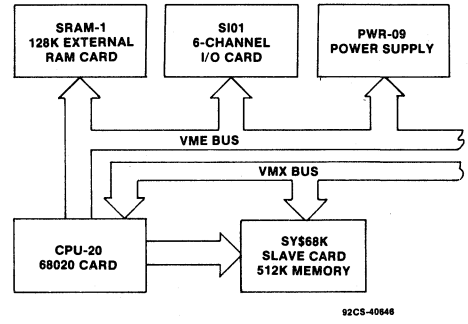


Fig. 1 - Block diagram of VME system.

STANDARD BIPOLAR LOGIC SYSTEM - UNMODIFIED

Tests Performed on the Operating System

The power on the 5-volt supply is monitored, and the system's major waveforms are recorded and compared to the published standards of the manufacturer. Built-in benchmark timing tests are used to verify system timing, access timing, and communication ability between the cards. Built-in tests, designed by the manufacturer, assure that the system is operating within the specifications. These tests allow the comparison of the unmodified system (which contains bipolar FAST and LSTTL) to the modified system (which contains ACL and High-Speed CMOS). The correlation of these timing tests is very important to the validity of this conversion experiment.

Comparison Tests - The following tests are used to compare the operation of the system before and after the conversion of the glue logic:

1. Benchmark Test 1 - Decrement long word in memory 10M times.
2. Benchmark Test 2 - Pseudo DMA 1K bytes 50K times.
3. Benchmark Test 3 - Substring character search 100K times.
4. Benchmark Test 4 - Bit test/set/reset 100K times.
5. Benchmark Test 5 - Bit matrix transposition 100K times.
6. Benchmark Test 6 - Cache test—128K program executed 1K times. (This test can only be performed on the main CPU memory because of the memory requirements.)
7. Monitoring the VME system clock.
8. Monitoring the major handshaking signals on the bus (DTACK, DATA VALID, DS"A" and DS"B") and comparing the results to the specifications both before and after conversion.
9. The 5-volt power supply is monitored with a clamp-on current probe to observe the change in both standby and operating power on the VME and VMX bus.
10. The bus waveforms are monitored to observe the signal reflections on the bus.
11. All critical waveforms are monitored for their signal reflections.
12. A test macro program is generated and its execution time is recorded and compared.

The tests were chosen to be as simple as possible (allowing the system designer to easily evaluate the modification) but still provide accurate testing of the system.

Standard Unmodified System Benchmarks and Specifications

Table II contains the critical timing specifications required and used in the test. Table III contains the results of the benchmark timing tests.

Table II - Critical Timing Specifications

Signal	Critical Specs.	Observed Specs.
Sys Clk	16.0000 MHz	16.0102 MHz
DS0 to DS1 skew	20 ns max	3 ns
Data Valid to DTACK	0 ns min	40 ns
AS to BTACK	20 ns min	30 ns

Table III - Results of Benchmark Timing Tests

Test	Timing Results (seconds)
Main Bd.	
Bench No.	
1	10.79
2	13.90
3	11.91
4	3.71
5	11.29
6	21.64

The system clock is shown in Fig. 2. The top waveform is monitored at the driver output while the bottom waveform is the system clock signal at the very end of the bus (at the I/O port card). All three cards are in the system, and signal reflections can be seen as three bumps when the signal is low. Each reflection is about 5 ns wide and about 0.75 volt above ground. As each card is removed, the number of reflections and the loading factor is reduced. Fig. 3 illustrates that there are less reflections and that the signal integrity has improved.

Fig. 4 shows the same effect, but with only the main card in the system. These reflections are from each input and the bus. If the reflection voltage exceeds the TTL switching threshold, false triggering will occur and system operation will be hampered.

Fig. 5 illustrates the signals of DS0 to DS1. Fig. 6 illustrates DATA VALID to DTACK. Fig. 7 illustrates AS to BTACK. These signals are detailed in Table III.

Power

The unmodified system consists almost entirely of bipolar-type logic: TTL, LSTTL and FAST, which are glue logic, plus many bipolar LSI and VLSI parts. Another large user of power is the VME resistor terminations, which are at either end of the bus. The system uses a full 32 bits with the option of either a 16 or 32-bit data bus. There is also the VMX bus, which extends the system for 32-bit operation and contains the same resistor terminations as the VME bus. A typical VME board is multilayer (a requirement because of the number of connections and the huge amount of power required to operate the circuits). Table IV shows the amount of power the unmodified system requires and each board's contribution.

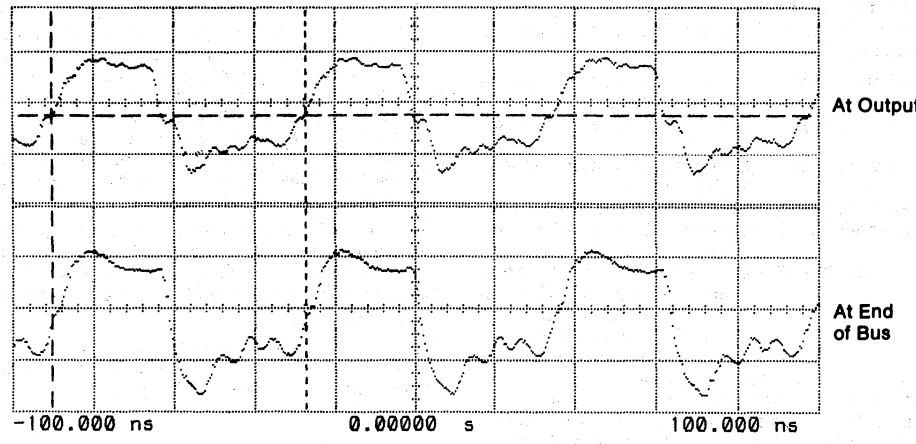
Table IV - System Power and Board Contribution

Item	Power - 5V (Watts) VME	VMX
CPU-20	14.25	7.05
SRAM-1	2.95	NA
SI/01	3.65	NA
Total	20.85	7.05
Total Operating Power (Data Access)	21.25	8.99

Total Power - 5V Supply: 27.9 Watts

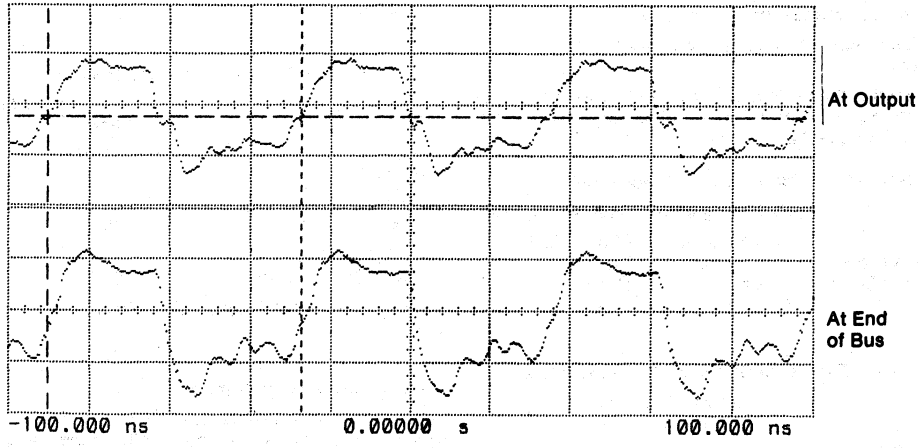
Unmodified-System Summary

The above tests and data show that the present system is in good working order, and that it follows the manufacturer's specifications. All of the above data will be used to compare the operation, performance and system integrity to the modified system (bipolar logic replaced with ACL and High-Speed CMOS). The unmodified system uses a very large amount of power. The modified system will reduce both the standby and operating power through the replacement of the glue logic; the LSI and VLSI parts in the system cannot be changed.



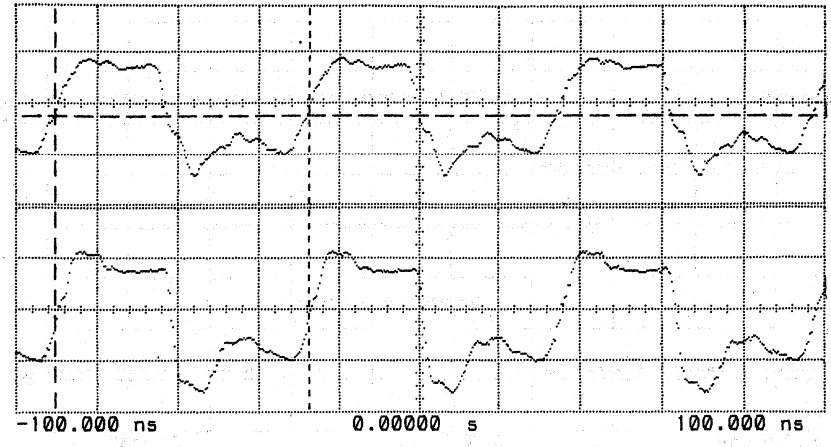
Ch. 1	= 2.000 volts/div	Offset	= 2.000 volts
Ch. 2	= 2.000 volts/div	Offset	= 2.000 volts
Timebase	= 20.0 ns/div	Delay	= 0.00000 s
Ch. 1 Parameters		Freq.	= 16.0051 MHz

Fig. 2 - Signal reflections, 3 cards.



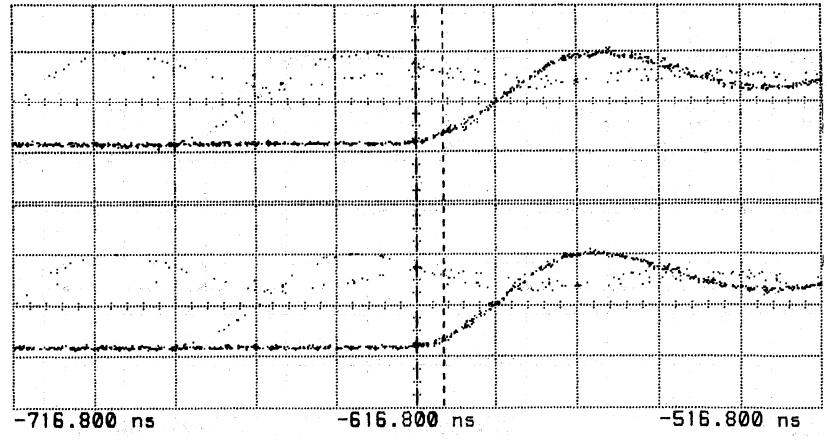
Ch. 1	= 2.000 volts/div	Offset	= 2.000 volts
Ch. 2	= 2.000 volts/div	Offset	= 2.000 volts
Timebase	= 20.0 ns/div	Delay	= 0.00000 s
Ch. 1 Parameters		Freq.	= 16.0051 MHz

Fig. 3 - Signal reflections, 2 cards.



Ch. 1	= 2.000 volts/div	Offset	= 2.000 volts
Ch. 2	= 2.000 volts/div	Offset	= 2.000 volts
Timebase	= 20.0 ns/div	Delay	= 0.00000 s
Ch. 1 Parameters		Freq.	= 16.0051 MHz

Fig. 4 - Signal reflections, 1 card.



Ch. 1	= 2.000 volts/div	Offset	= 2.000 volts
Ch. 2	= 2.000 volts/div	Offset	= 2.000 volts
Timebase	= 20.0 ns/div	Delay	= -716.800 ns
Delta T	= 6.800 ns		
Start	= -616.800 ns	Stop	= -610.000 ns

Fig. 5 - DS0 to DS1.

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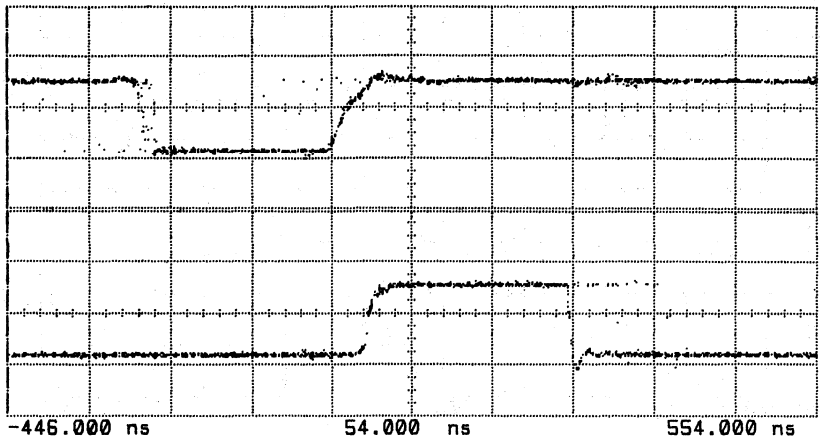
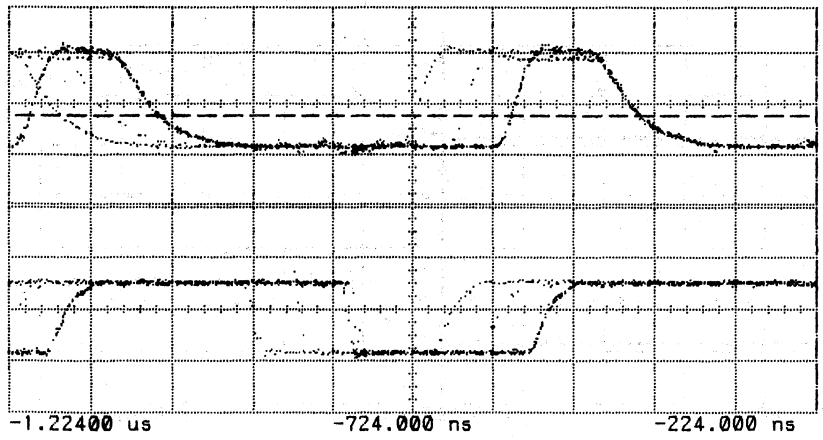


Ch. 1 = 2.000 volts/div		Offset = 2.000 volts	
Ch. 2 = 2.000 volts/div		Offset = 2.000 volts	
Timebase = 100 ns/div		Delay = 54.000 ns	
Delta T = 6.800 ns			
Start = -616.800 ns		Stop = -610.000 ns	

Fig. 6 - Data valid to DTACK.



Ch. 1 = 2.000 volts/div		Offset = 2.000 volts	
Ch. 2 = 2.000 volts/div		Offset = 2.000 volts	
Timebase = 100 ns/div		Delay = -724.000 ns	
Delta T = 83.520 ns			
Start = -1.520 ns		Stop = 82.000 ns	
Delta V = 0.000 volts			
Vmarker1 = 1.540 volts		Vmarker2 = 1.540 volts	

Fig. 7 - AS to BTACK.

MODIFIED SYSTEM DATA

This section of the Note deals with the replacement of the bipolar glue logic with Advanced CMOS Logic and High-Speed CMOS parts. It consists of a comparison of timing, signal integrity, waveforms, and power savings of the unmodified system with the modified one.

The same tests as those used in the unmodified system will be performed and their results recorded for comparison. The test results must be within the manufacturer's specifications to prove the modification successful.

Modification Procedure

In replacing the glue logic, the specifications of the ACL and the High-Speed CMOS parts must be met. The system schematic must be reviewed, and only those parts that can be operated within specification can be substituted. The VME bus specification states that each driver must be able to sink a total of 64 mA at 0.5V. ACL can only sink 24 mA at 0.4V. For the purpose of this experiment, the VME bus in the system is limited to 1 backplane and terminations at either end only. This restriction keeps the operation to within the limits of ACL and allows the replacement to be carried out.

Each card is reviewed and modified with the correct logic. FAST is replaced with AC, and LSTTL is replaced with HCT High-Speed CMOS logic. The AC type logic is used because the signal inputs are at CMOS levels, or unloaded TTL outputs pulled up to at least 4.25, which is above the V_{IH} of 3.5V of the AC specification, and most of the glue logic is associated with the data buses. HCT High-Speed CMOS is used to replace LSTTL because of its ability to switch on TTL levels; most of the LSTTL ICs interface to bipolar LSI and VLSI.

ALS is also present in the system, mainly in the external card's VME bus interface. The ALS 645-1 has a higher current-sink capability than normal ALS. For the purpose of this paper, the ALS 645-1 and 641-1 are being replaced by the AC245 and the AC241. These AC parts have the same pinout and function with the increase in speed of ACL. The ALS drivers are directly connected to the VME and VMX buses, which for this experiment are being limited to the restriction stated above.

Standard Modified System Benchmarks and Specifications

Table V contains the critical timing specifications monitored, and compares them to the unmodified system. Table VI contains the results of the benchmark timing tests. The above tests show that there are few or no timing changes between the modified and unmodified units. The only difference, which should not effect system timing, is that CMOS logic will give the user a more even propagation delay than bipolar logic, and a larger output-voltage swing.

Table V - Critical Timing Specifications

Signal	Critical Specs.	Observed Specs.
Sys Clk	16.0000 MHz	16.0359 MHz
DS0 to DS1 Skew	20 ns max	2.5 ns
Data Valid to DTACK	0 ns min	40 ns
AS to BTACK	20 ns min	29 ns

Table VI - Results of Benchmark Timing Tests

Test (Bench No.)	Timing Results (seconds)
1	10.79
2	13.90
3	11.92
4	3.71
5	11.29
6	21.65

Waveforms

The system clock is shown in Fig. 8. The top waveform is monitored at the driver output, and the bottom one at the end of the bus (I/O card). All three cards are in the system, and the signal reflections from each card can be observed in the waveform during a low. The output voltage swing is higher due to the rail-to-rail swings of the CMOS technology. The signal integrity is similar to that of the unmodified unit. Each reflection can be seen, as mentioned above. Fig. 9 shows the system clock with only two cards present.

Fig. 10 shows the clock with only the main card present in the system. The clock signal has balanced high and low pulse widths. By using logic with CMOS thresholds, the noise margin of the bus and the system can be improved. Noise immunity in a TTL-type logic system is limited because of the lower switching thresholds. The unmodified system noise reflections approach the 0.8V TTL logic-low window.

With CMOS input devices, the typical 50% switching threshold provides the designer with a larger noise window than the TTL types. The larger CMOS signal output is thought to produce a larger EMI, RFI, and dv/dt than the signal output which TTL logic produces. Observations in this system show that the total RFI and EMI is about the same because of the lower power consumption, which is discussed in the next section.

Power

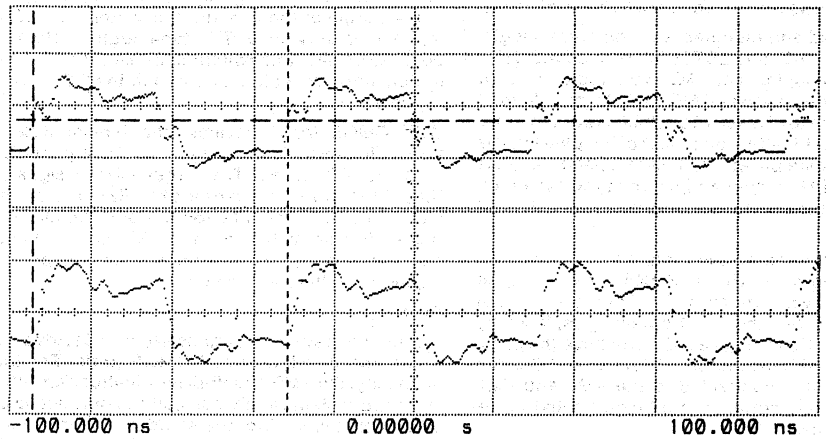
The modified system contains a total of 51 Advanced CMOS Logic and 21 High-Speed CMOS parts. For the sake of simplicity, the VME and VMX terminations are left the same. In a VME system which, basically, is only active on the bus when communicating, the standby power consumption is very high because of the large quiescent current required by the bipolar logic. The modified system replaces this logic with CMOS, which has almost no quiescent current requirements, it only consumes power when switching. Even though the bipolar LSI and VLSI cannot be replaced, there is still a substantial power reduction in the system. Table VII shows the power measured in the system after the conversion.

MODIFIED SYSTEM SUMMARY

The modified system demonstrates the many reasons for using CMOS instead of power-hungry bipolar logic. Overall system operations and timing are not effected by the change, but power dissipation clearly drops. The significant power reduction highlighted by the above data clearly points out the reasoning behind and advantages to a conversion to CMOS logic. The conclusion of all of the above data is that CMOS logic (ACL and High-Speed CMOS) is far superior in standby power dissipation, noise margin, and reliability to bipolar types, and should be the first choice in system replacement or new designs. Moreover, the VME and VMX buses, which require a large power dissipating termination, should be redefined for use with CMOS logic and to reduce power use in systems, thereby improving reliability and lowering system cost.

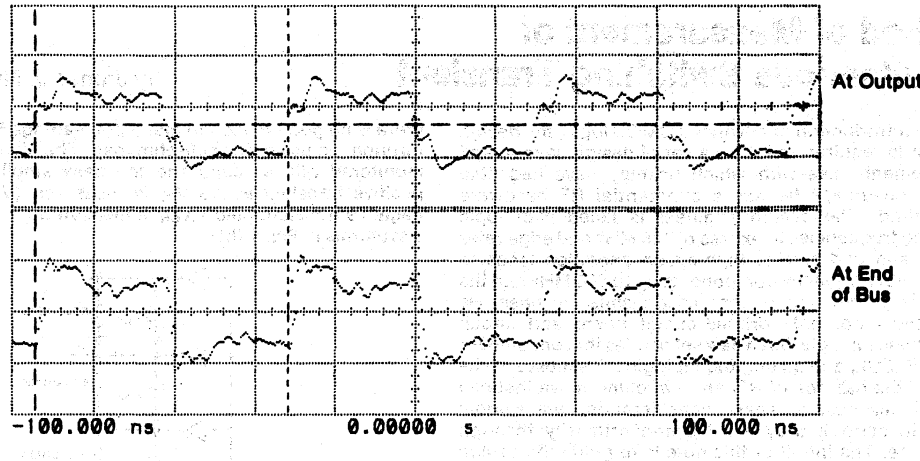
Table VII - Power Measured After Conversion

Item	No. of ICs Replaced FAST	LSTTL	ALS	Power (5V) (Watts)		Savings over Bipolar (Watts)	
CPU-20	30	0	7	VME:	9.9	VMX:	4.35
	1	6	7	VMX:	4.4	VMX:	2.65
SRAM-1	0	15	6	VME:	0.62	VMX:	2.3
SI/O1	31	21	20	VME:	3.13	VMX:	0.52
Total System				VME:	13.65		
				VMX:	4.4		
Grand Total					18.05		9.85 45%
Total System (Data Access)				VME:	19.00		
				VMX:	5.50		
Total ICs Replaced: 72							



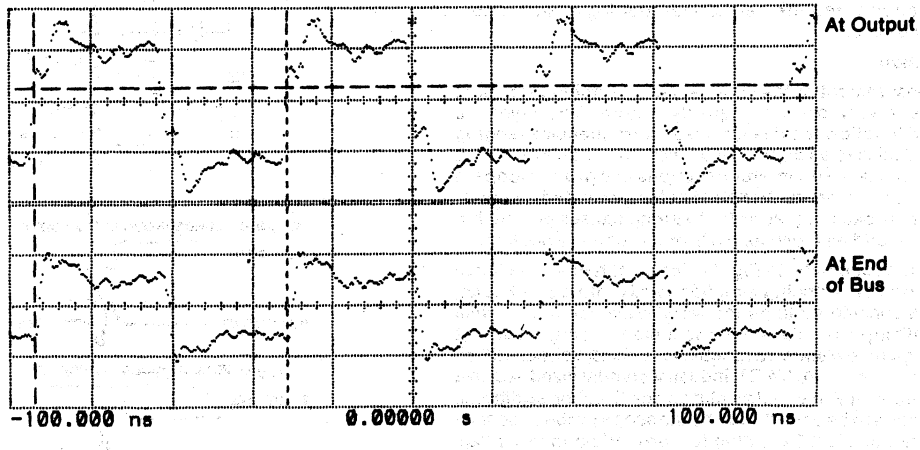

```
Ch. 1      = 4.000  volts/div        Offset     = 4.000  volts
Ch. 2      = 4.000  volts/div        Offset     = 2.800  volts
Timebase   = 20.0 ns/div             Delay      = 0.00000  s
Ch. 1 Parameters                     Freq.      = 15.9642 MHz
```

Fig. 8 - Signal reflections, 3 cards.



Ch. 1	=	4.000 volts/div	Offset	=	4.000 volts
Ch. 2	=	4.000 volts/div	Offset	=	2.800 volts
Timebase	=	20.0 ns/div	Delay	=	0.00000 s
Ch. 1 Parameters			Freq.	=	15.9668 MHz

Fig. 9 - Signal reflections, 2 cards.



Ch. 1	=	2.000 volts/div	Offset	=	2.760 volts
Ch. 2	=	4.000 volts/div	Offset	=	2.800 volts
Timebase	=	20.0 ns/div	Delay	=	0.00000 s
Ch. 1 Parameters			Freq.	=	16.0359 MHz

Fig. 10 - Signal reflections, 1 card.

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ICAN-8754

Method of Measurement of Simultaneous Switching Transient

by James J. Nadolski

With the introduction of advanced CMOS logic, the design engineer is required to follow a set of design, layout, and measurement rules with which he may have had little experience unless he has a substantial RF hardware background. The design engineer is faced with logic operating frequencies in excess of 125 MHz and edge rates of 5 ns and under. This high-speed operation leads to dealing with frequency components up to 500 MHz and the treatment of interconnections as transmission lines. He must follow not only printed-circuit board and circuit design rules for logic, but a new set of rules that encompass logic, RF, ECL, and analog technologies. He must also be aware of the hazards of RFI and switching noise that can occur in his design. These considerations are seldom taught in school; they are learned primarily through experience. The intent of this note is to guide the design engineer in the preferred method of measurement of the simultaneous switching transient, which also goes by the name "ground bounce effect". This measurement is difficult for accuracy and repeatability because it is an RF type of a measurement and many variables come into play that are masked in logic systems of lower speed and longer transition time. The following information and test methods will permit the engineer to measure this transient accurately and with repeatability. Topics discussed include an example of a good RF quality test fixture, proper equipment, best and worst case V_{OLP} measurement, test circuit schematics, power supply requirements, methodology, and actual measured data.

Preparation

The measurement of the simultaneous switching transient requires a very good RF quality fixture. The layout is required to follow the design rules for frequencies ranging from 100 MHz to as high as 500 MHz. The fixture must add minimal noise due to interconnections and ground loops in order to not distort the transient pulse generated by the IC chip and its package. Poor RF fixturing causes ground lift, which can add as much as 0.5 V or more to the reading.

The circuit schematic in Fig. 1 is for octal types. It includes seven outputs switching simultaneously into a 50-pF load, which is considered to be the worst-case condition, while the eighth input is held either low or high placing the output into a high or low state, respectively. This test circuit (50 pF + 500 ohm) is the AC/ACT industry standardized AC test load. The 47-pF capacitor allows for 3 pF of additional capacitance to be contributed by the scope probe or coaxial connections. GE/RCA testing for "ground bounce" or V_{OLP} is performed for the worst-case conditions without the 500-ohm load that discharges some of the stored capacitor energy externally and not through the IC ground return path, which is significant. Inclusion of the 500-ohm resistor would unnecessarily decrease the maximum V_{OLP} reading by about 50 mV. Because CMOS inputs are purely capacitive, there is no good reason to make the readings 50 mV lower through the use of the 500-ohm load. The eighth output is monitored with a scope and the peak amplitude of the positive transient above V_{OL} is measured (V_{OLP}); or the negative transient below V_{OH} is measured (V_{OHV}). See the waveforms in Fig. 1 (b).

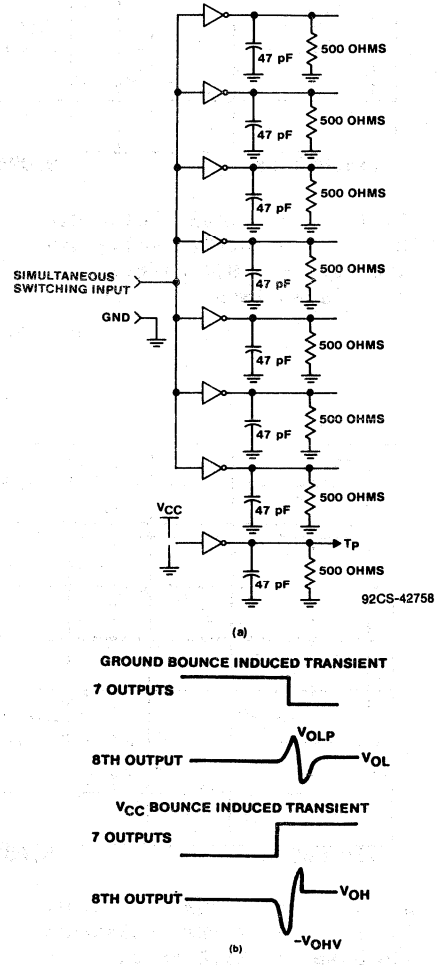

Fig. 1 - Test circuit and waveforms of simultaneous switching transient (ground bounce).

The major concern of the design engineer is the V_{OLP} or low output level. Tolerance of this noise voltage is highly dependent on the switching threshold and noise margin of the logic circuits connected to the output of the device. With the CMOS switching threshold (typically 50% of V_{CC}) there is usually not enough energy in this pulse to cause false switching. More critical is when the logic inputs connected to the device switch at TTL thresholds (typically 1.5 V). Consequently, in order to generate V_{OLP} data as accurately as feasible, deletion of the 500-ohm external capacitor discharge load is recommended.

Fixture Layout and Design

The fixture used in the testing of "ground bounce" is designed to be as simple and low cost as possible but follows some elementary RF rules. The printed circuit board (PCB) is double-sided glass epoxy made of FR-4 material, 2-ounce copper, with no solder mask. At these frequencies the solder mask could add leakage paths to the PCB. One side of the PCB is primarily ground plane; the other side handles the very short connections from the IC pins to the load capacitors. The value of the load capacitors is 47 pF. The total load capacitance per output is 47 pF plus 3 pF of stray capacitance for a total of 50 pF. The capacitors should be either the monolithic ceramic type with very short leads or chip capacitors. If 500-ohm resistors are also used, chip resistors are recommended. The layout of the PCB is shown in Fig. 2.

The IC under test is soldered into the board to minimize any added inductance, which sockets or socket pins would cause, thus exactly duplicating the inductance of the preferred application connection. The signal input to the board is terminated in 50 ohms to match the output of the pulse generator. Driving seven inputs with one pulse generator has the advantage of providing essentially no skew between the seven simultaneously switched stages. However, the seven stages load the pulse generator and increase the input rise time a little, but it is kept well under 3 ns, which is the recommended input rise time. The alternate would be to use seven synchronized pulse-generated signals, which would tend to make ground bounce readings appear lower because of the spreading of the switching currents of the seven individual stages due to some skew between the seven drive pulses. Power supply leads into the board must be kept as short as possible and twisted. The +5-volt supply is bypassed by both an electrolytic and a ceramic capacitor. The V_{CC} pin of the IC is also bypassed with a 0.1-μF ceramic capacitor. These precautions are necessary to minimize any effects of poor transient regulation in the power supply. Fig. 3 is the schematic of this recommended PCB worst-case ground bounce fixture.

During the assembly of the fixture, the least possible amount of solder should be used on each joint. The PCB should be cleaned well to remove all remaining flux. The output at which the ground bounce measurement will be taken should use a probe tip jack, with the ground of the

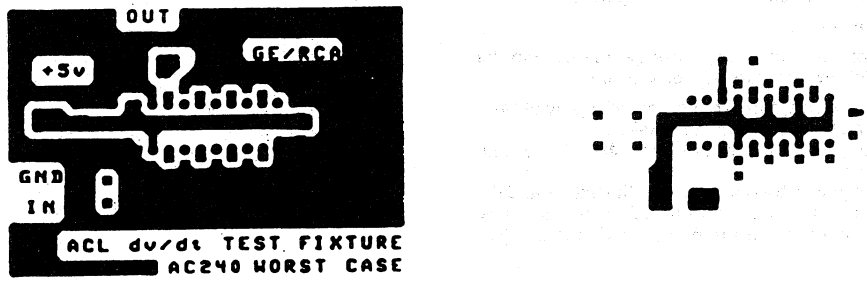

Fig. 2 - Physical layout of PCB test fixture.

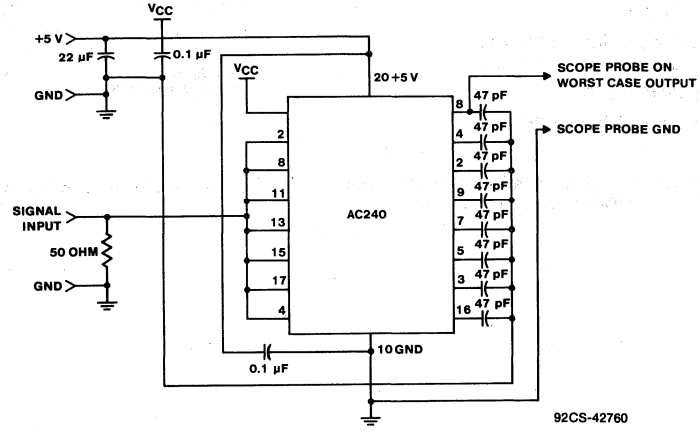

Fig. 3 - Schematic of ground bounce test circuit (worst-case condition).

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jack referenced to the ground pin of the IC and the tip of the probe right at the output pin. This arrangement avoids any ground loop effects. If the proper probe is not available, the use of direct connections to the scope through a 50-ohm coaxial cable in series with a 450-ohm resistor is an alternative technique providing correlation within about 50 mV. The reduced loading of the 10000-ohm, 2-pF probe is considered more "real world" for high-impedance CMOS transient environments.

Equipment Required and Setup

1. The power supply must have good transient regulation so that the supply rails do not move around during switching. The supply should have added bypass capacitance at its output terminals of 1000 μF in parallel with a 0.1-μF ceramic disk to prevent any added ground bounce resulting from poor supply regulation.
2. The pulse generator should have a 50-ohm output and a rise and fall time of under 3 ns measured at the input of the device under test in place. The switching test frequency is set to 1-MHz output frequency.
3. The scope bandwidth should be at least 750 MHz and active probes with a similar bandwidth specification are required because of the edge rates.
4. A digital voltmeter with resolution down to 10 mV should be used to monitor the power supply voltage set for the reading.
5. A digital thermometer should be used to record the ambient temperature at the time of reading. The reading of ground bounce changes with temperature because the gain of MOS ICs changes with temperature.

Measurement Technique

The power supply, oscilloscope, pulse generator, and the meters should follow this warm-up procedure.

1. To allow for any drift, turn on the power supply at least one-half hour before the reading is taken.
2. Set the pulse generator output to a 1-MHz, 5-V output into a 50-ohm load.
3. With the pulse generator connected to the fixture and the test IC in place, adjust the rise and fall time to 3 ns or less.
4. Measure and record the ground bounce due to the PCB alone.

Type: AC240

Worst-Case Value	1.06 volts
Best-Case Value	0.72 volts

Type: FAST F240

Worst-Case Value	1.05 volts

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Fig. 4 - Measured values of V_{OLP} made on an AC240 Octal-Buffer Line Driver, 3-State device and on a FAST F240.

A good PCB from the standpoint of ground bounce should have a bounce voltage of under 100 mV measured directly at the IC ground return pin. The actual ground bounce effect, measured at the 8th output pin under test, includes this PCB ground bounce component.

All measurements of ground bounce used for comparison purposes should be taken under the same conditions; the power supply voltage, pulse generator frequency and transition time should be identical. The ambient temperature should be identical within 3 degrees C because logic speeds and RF leakage change with temperature.

Example Measurements

Fig. 4 gives results of ground bounce tests made on Advanced CMOS Logic types using the above fixture and methods. Tests were run on both the best-case output pin (closest to the IC's ground pin) and the worst-case output pin (the pin furthest from the ground pin). A comparison with a FAST 240's worst-case output pin was also made. Fig. 5 shows these results in detail as displayed on the oscilloscope.

It should be noted that the measurement of ground bounce is a difficult and time-consuming task, but accurate and reliable measurements can be made by following the above recommendations. Differences in the readings from IC to IC can be ± 200 mV. Any comparison of IC's should take this variation into consideration.

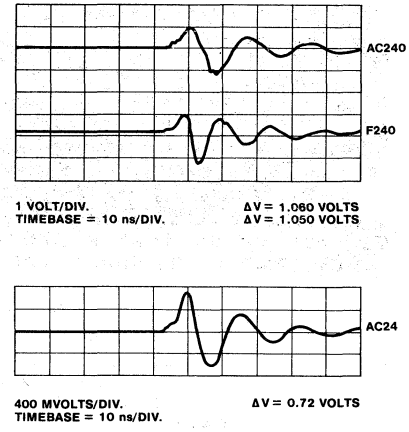

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Fig. 5 - Simultaneous switching transient waveforms.

FCT CMOS Logic Optimized for Backplane Interface

By W. Austin and B. Petryna

We are now at a new threshold in CMOS design capability, adding enhancement features and modifying the basic technology to support bipolar adaptations. Our purpose in this Note is to look at bus drive requirements and the advantages to be gained by applying these new techniques to a modified CMOS structure. A newly developed RCA FCT logic design is primarily a CMOS structure having the advantages needed to drive a VME-bus backplane bus.

Much has been said about the advantages of Advanced High-Speed CMOS Logic devices as bus drivers for a VME bus or equivalent bus system. The basic advantages of CMOS in any high-performance system application are well known. The speed capability developed in the new families of AC/ACT and FCT is now second only to that of the ECL and GaS technologies. The classic qualities of CMOS low-power consumption and excellent noise immunity cannot be overstated. The wide operating-temperature range of CMOS with minimal change in electrical characteristics is important to the performance and reliability of any system. These merits have been demonstrated in HC/HCT versus LSTTL logic and AC/ACT versus FAST logic. These qualities are retained in the latest RCA FCT logic circuits.

VME-Bus Conditions

While the specifications for a VME bus, such as the one illustrated in Fig. 1, are defined for bipolar integrated circuits, no restrictions are placed on the use of any technology that can produce equal or better results. The application techniques for AC/ACT logic driving the VME bus or an equivalent data bus system have been explored. AC/ACT logic does have considerable application potential,

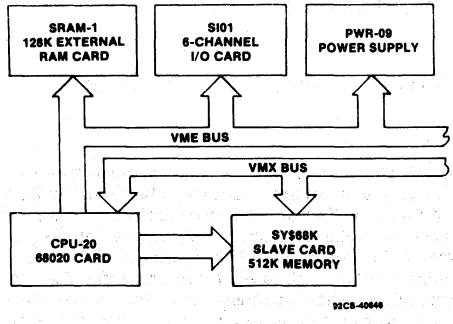

Fig. 1 - VME-bus system block diagram.

but also has limited drive capability. AC/ACT logic is defined for 24-mA sink and source drive, while the VME-bus specifications call for 48 and 64-mA sink current to drive several of the backplane lines. The VME bus may have as many as 21 slots spaced over 500 mm (19.7 inches), with 2 pF (no load) to 20 pF per slot. The combined capacitance loading and low characteristic impedance of each bus "stripline" gives rise to the need for high current drive to support the high-speed data rates of the bus.

The bus tolerance specifications for power-supply voltage are relatively tight, giving rise to another bus design problem. It must be recognized that imbalance in power supplies does exist. Imbalance may occur with deteriorating conditions of contact resistance or separate system power-supply changes and any irregular conditions that produce transients on the line. The imbalance, if sufficient, can overdrive protection and substrate diodes at the input and output of CMOS devices. While the problem can be resolved by various design techniques, "bus hang-up" resulting from power-supply imbalance can be resolved more directly by the use of RCA FCT logic circuits. On-chip circuit design features include current-blocking diode junctions to prevent differential-power-supply imbalance problems.

A VME-Bus Model

The VME-bus lines may be characterized by a given set of modeling information. As shown in Fig. 2(a), if we use a microstrip circuit element 0.1 inch in length, each PC board microstrip element of line has 0.129 pF of shunt capacitance and 1.561 nH of series inductance, for which the line characteristic impedance (Z_o) is:

$$Z_o = (L/C) \text{ exp } 0.5$$
$$= (1.561 \text{ nH}/0.129 \text{ pF}) \text{ exp } 0.5$$
$$= 110 \text{ ohms}$$

And, as a model to determine drive requirements, a slot-to-slot segment consists of eight sections of the 0.1-inch element. If we include the 2 pF per empty slot on the VME-bus line as a distributed capacitance, the Z_o becomes 64 ohms. VME-bus rules state that the characteristic impedance for each unloaded "microstrip-line" is recommended to be approximately 100 ohms, not including slot capacitance loading. The backplane as a line may be configured by choice as end driven or center driven, although some slot positions, such as the system clock driver (specified to slot no. 1) are predetermined. Various configurations are shown in Figs. 2(b) and 2(c). For the purposes of modeling, the slot load is identified as an occupied slot with the characteristics shown in Fig. 2(d).

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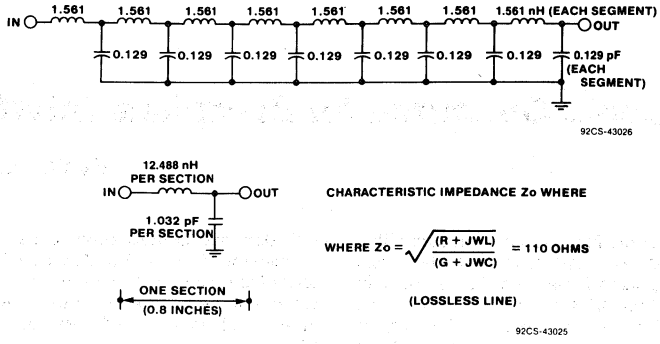

Fig. 2(a) - Cascade of 0.1-inch microstrip-line elements used to simulate each 0.8-inch of a slot-to-slot line segment.

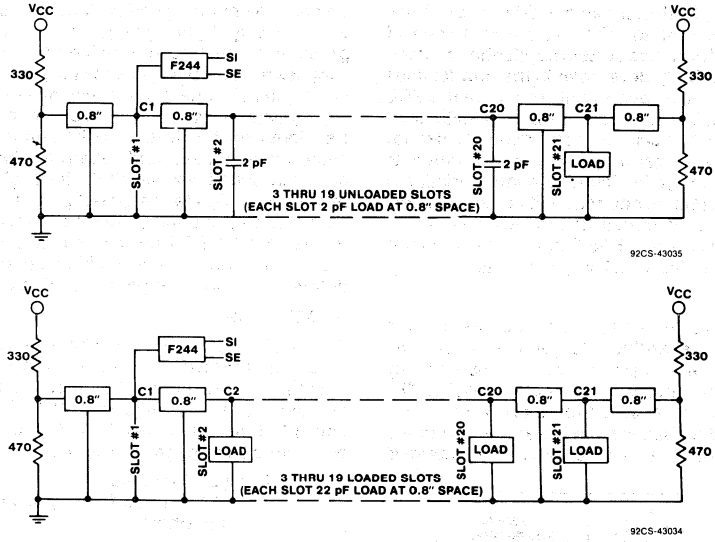

Fig. 2(b) - Test-circuit simulation model for an end-driven VME-bus line: unloaded (top) and loaded (bottom).

While the configuration described in Fig. 2 was established for modeling, it is our intent here to note the performance of the RCA FCT versus AC/ACT and FAST line drivers in this representative system. Using a defined number of slots as loads on the VME bus, the performance characteristics of the RCA FCT line drivers in a VME-bus application are shown.

The line terminations are defined for both ends of the VME bus as 330 and 470 ohms in series or a Thevenin equivalent of 2.94 volts and 194 ohms. It is readily apparent that the resistive load is a major concern for power requirements on the bus. FCT and CMOS bus drivers may be designed to have only a few ohms of channel resistance to meet the bus drive-level requirements and, by the defined standard, imitate the bipolar characteristics as a bus driver. The standard VME-bus termination is shown in the circuit of Fig. 3.

As noted, when capacitance is added at the distributed slots in the backplane, we are effectively changing the Z_o of the line. With more distributed line capacitance, the Z_o of the line is lower, making the line termination a greater (higher) mismatch in impedance. This increased mismatch, and irregular loading, will cause more line reflections. It is a primary concern here to show that the reflections, as well as ringing and other noise on the line, does not exceed a specified level of noise immunity while still meeting the timing requirements of the line. The device selected to demonstrate the VME-bus drive capability is the FCT 240. The structure we have chosen for demonstration is a standard VME backplane with nine slots filled. A block diagram of the test fixture is shown in Fig. 4.

Differential Power-Supply Problems

Power-supply imbalance on the VME bus may cause the bus to hang up when drivers operate from unequal power-

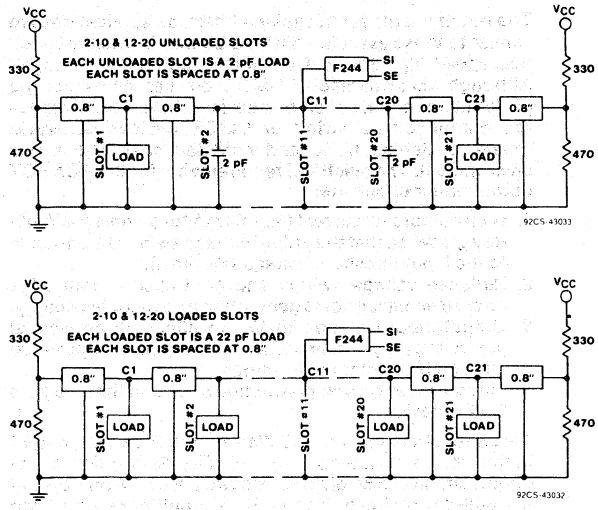

Fig. 2(c) - Test-circuit simulation model for a center-driven VME-bus line: unloaded (top) and loaded (bottom).

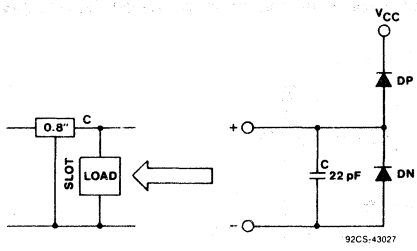

Fig. 2(d) - CMOS-equivalent slot load on the bus line.

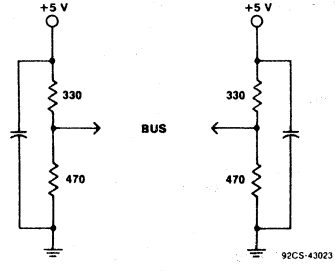

Fig. 3 - Standard VME-bus termination.

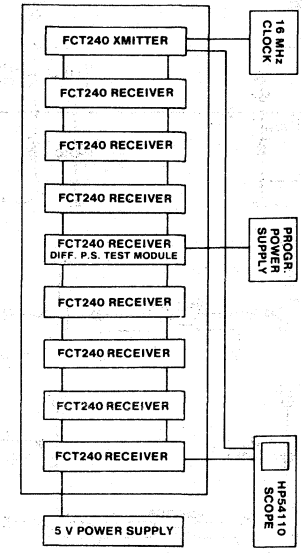

Fig. 4 - Block diagram of the VME-bus backplane test chassis.

supply levels across the length of the bus. For obvious reasons, the specifications for the power supplies must be very tight. The bus tolerance specification for the +5 volt supplies are +0.25/-0.125 volt. However, under stress conditions with added voltage drop in the contacts and lines, it is probable that some switching conditions will cause the line voltage to exceed the standard power-supply tolerance and the nominal IC specification of V_{CC} + 0.5 volts. Nearly all computer systems have board-to-board or frame-to-frame power-supply differences, which can cause bus-driver problems. There are various ways to accommodate this imbalance, such as the use of diodes to prevent excessive current when on-chip diode junctions are reversed. Where AC/ACT or HC/HCT CMOS is used, the common technique illustrated in Fig. 5 may be used to prevent reverse current through the IC.

While line drivers may be designed with CMOS technology to meet all specified signal switching levels for the VME bus, and avoid power supply problems by using the blocking diodes of Fig. 5, the technique may be regarded as a problem fix and not a design solution. All line receivers or operational transceiver devices require the protection because of the potential problem at the receiving end of the line. Drawbacks are noted with the use of diodes, such as the need for low forward-voltage drop equivalent to the Schottky barrier diodes. The diode adds to the power-supply tolerance problems and reduces the noise immunity of the system. Still, this does not change the fact that standard CMOS designs have input and output diodes that will reverse when overdriven. And, without protection, the condition of overdrive on the bus can cause hangups and timing-delay problems, as well as overdissipation.

The design of RCA FCT output driver structures includes protection to prevent driver interfaced loading on the bus during wide ranging of power-supply differential voltage. Given a separate supply for an FCT-loaded line driver, variations of zero to maximum V_{DD} will not cause the backplane line to be loaded. Measurement results verify the design goals as noted above.

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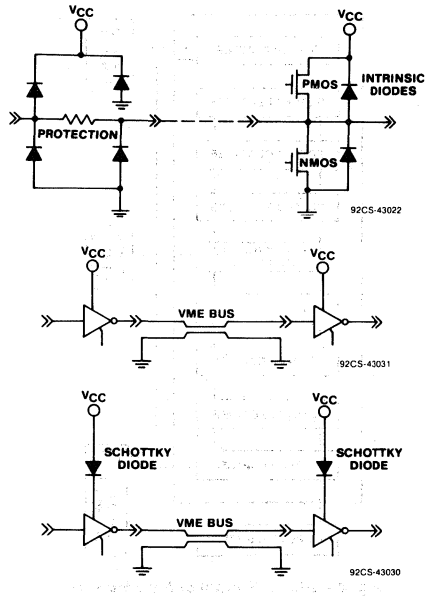

Fig. 5 - AC/ACT driver interface to the VME bus with Schottky-diode recommendation to solve differential power-supply problem.

RCA FCT Circuit Description

The requirements for backplane interface applications are similar to those associated with a bipolar transistor circuit (i.e., speed, high drive current, and limited voltage swings). Although small geometry CMOS devices can meet the performance criteria of bipolar devices, the inherent rail-to-rail output-voltage swing of CMOS devices generates greater switching noise and reflected energy in a bus environment. The electrical requirements for the RCA FCT output buffer circuit are:

1. High output sink current (I_{OL} = 64 mA for commercial/military grade) so that the output voltage swing is monotonic to the input threshold voltage (V_{IL} max.).
2. Reduced voltage swings and controlled output edge rates to minimize noise generation and reflected energy.
3. Output/Input isolation to V_{CC} to eliminate differential power-supply problems where devices may be powered through input/output structures.
4. Low quiescent power dissipation similar to that of a pure CMOS device.

These requirements are satisfied by the RCA FCT output buffer design illustrated in Fig. 6. The description of the output circuit can be divided into two parts, the pull-up and the pull-down circuit. The pull-up circuit consists of two active elements, an NMOS and n-p-n transistor. The NMOS transistor is the switching element that pulls the output from the V_{OL} through the output switch point (1.5V). The n-p-n transistor is the output-voltage-level element that limits the V_{OH} level to 2 V_{BE} below the supply voltage. This pull-up circuit configuration isolates V_{CC} from the output. The pull-down circuit consists of a distributed NMOS, which is turned on sequentially to control the switching current transients and the output skew rate (dv/dt). This control is combined with a limited voltage swing to minimize switching noise and reflected energy on the backplane.

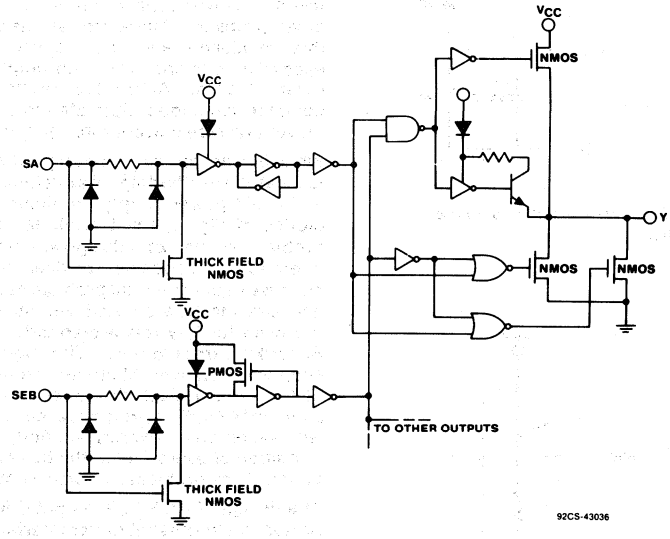

Fig. 6 - Logic diagram of the RCA FCT driver circuit.

Measured Drive Data

To establish measured capability for the simulated FCT VME bus driver, the simulation curves of Fig. 7(a) were run with alternate slots loaded to show significant points of comparison in typical curves. Theoretical results show that the end of the line drives to a higher level than the input if the matching impedance is higher than the characteristic impedance. This is the case in Fig. 7(a) where slot 21 shows

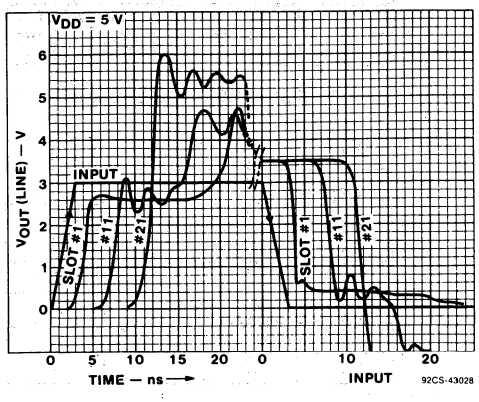

Fig. 7(a) - VME-bus simulated curves for typical conditions with loading in the odd-numbered slots.

levels rising to an overshoot of more than 5 volts with some ringing. It is for this reason that FCT switching levels are typically 3 volts. Similar results occur in the negative step as the output goes below the ground level, but is otherwise clamped by the load diodes. Fig. 7(b) is added to show a fully loaded VME bus; waveforms are shown for slots 1, 11, and 21. This is a worst-case condition for the same simulation parameters used to drive the bus. Due to the added loading, the overshoots are less, but the settling time is longer. It should be noted that a fully loaded bus is not common design practice because of close spacing and mechanical size limitations.

Another significant point of comparison is the initial and final settling levels of the input step for both directions of

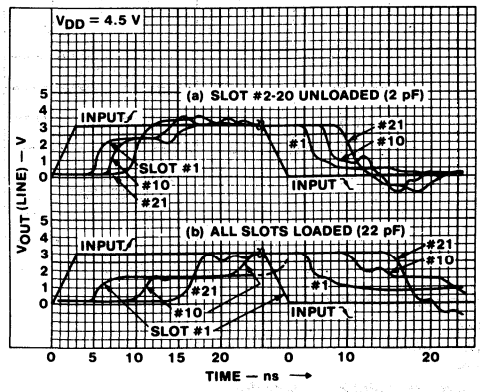

Fig. 7(b) - Worst-case VME-bus simulation plots: unloaded (top) and all slots loaded (bottom).

switching. On the rising edge of the pulse, an initial setup level of change occurs before finally settling to the high pull-up level. This transitional change is less as we move further down the bus line. When the change is in the negative direction, similar undershoot or overshoot occurs, depending on the position on the line. Sufficient drive requirement is needed at line drive input to pull the negative transition firmly to ground without a ringing bounce on the line. The initial step change must stay below the specified V_{IL} level for TTL, a condition that may be difficult to meet if the driver is not designed for 64 mA of sink current.

Measured comparisons of FCT240, F240, ACT240, and IDT240 drivers are shown in Figs. 8 through 11, where 8(a), 9(a), 10(a), and 11(a) show loaded (see Fig. 4) and 8(b), 9(b), 10(b), and 11(b) unloaded conditions. In this set of measurements, the VME bus chosen for test had resistive-load terminations in slots 1 and 21, a driver in slot 2, a receiver in slot 20, and loads in the even slots, but no plug-in module at slot 16.

The FCT240 data is similar to that of the simulated condition, but with less ringing and at a lower frequency. The rise-time edge rates for all waveforms are much less than the normal delay time for the VME bus as shown, which is about 8 ns loaded and 5 ns unloaded. The rising edge exceeds the 5V supply level to about twice the input drive level; similar conditions on the falling edge show a negative transition to about -1 volt. Protection diodes at the input provide clamping, which dampens any negative swing.

The F240 curves of Figs 9(a) and 9(b) show similar results except for more damped conditions due to the input loading characteristic of the bipolar devices. The rise time is somewhat slower than the FCT and the propagation delay is noted to be essentially the same as for the FCT. In general, the F240 and FCT240 have similar characteristics except for the faster rise time and the peak voltage swing for the FCT device.

The performance of the ACT device is shown in Fig. 10 for comparison. The performance of the ACT240 is similar to the F240 and FCT240 for the VME-bus test fixture used. Under the loaded conditions shown, the trailing edge is slower to settle to zero. The rising edge pull-up is much stronger, which for most switching applications is an advantage. As a driver for the VME bus, under loaded or loaded-line conditions, the ACT output reaches a level of 7.5 volts. This value is marginally over the maximum V_{DD} ratings. The use of a dropping diode in the V_{DD} line should serve as a means to keep the maximum positive level within ratings, as well as to resolve any differential-power-supply system problems.

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3. "Powering VME-Bus Systems," W. Yates, Electronics Products, Jan. 15, 1988.

Acknowledgments

Measurement data taken by E. Wittmann; circuit modeling and simulation data done by C. Hsu.

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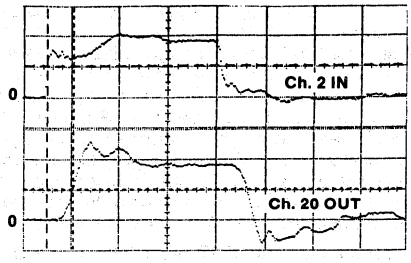


Fig. 8(a) - RCA FCT240 loaded.

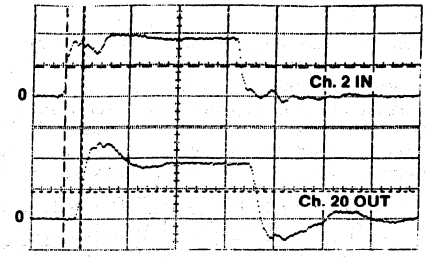


Fig. 8(b) - RCA FCT240 unloaded.

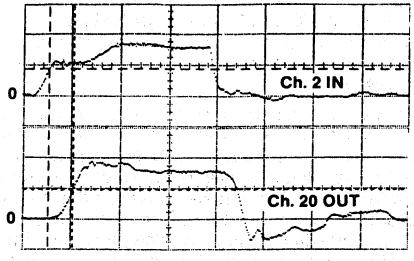


Fig. 9(a) - F240 loaded.

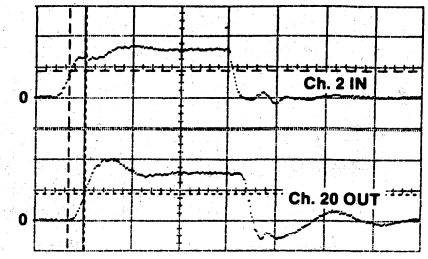


Fig. 9(b) - F240 unloaded.

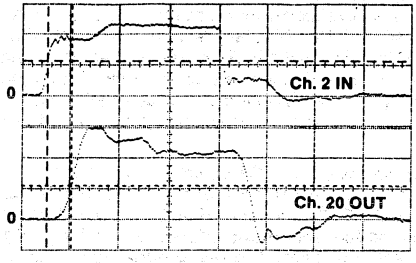


Fig. 10(a) - RCA ACT240 loaded.

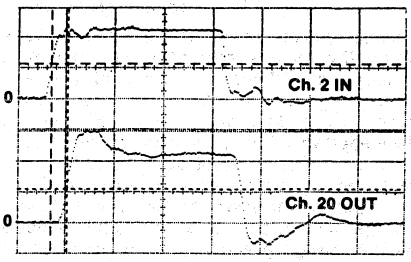


Fig. 10(b) - RCA ACT240 unloaded.

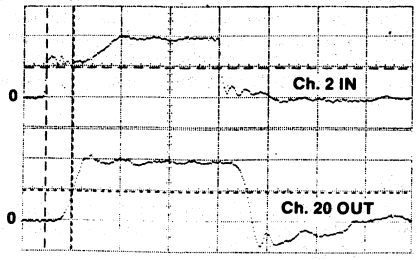


Fig. 11(a) - IDT 240 loaded.

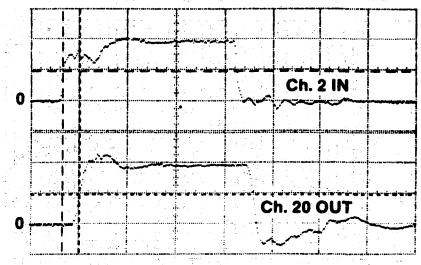
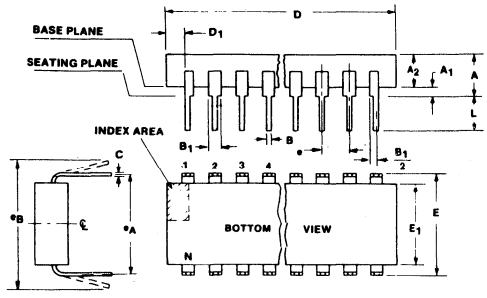


Fig. 11(b) - IDT 240 unloaded.

Figs. 8 to 11 - VME-bus measurements comparing line drivers (Fig. 4 test fixture):
Channel 1 (top) = 2.5 V/div (vertical)
Channel 2 (bottom) = 2.5 V/div (vertical)
Timebase = 15.0 ns/div (horizontal)
(a) Backplane with even slots loaded; driver slot 2 (top waveform);
receiver slot 20 (bottom waveform)
(b) Backplane with slots 3 to 19 unloaded; driver slot 2 (top waveform);
receiver slot 20 (bottom waveform).

Dimensional Outlines

Dual-In-Line Plastic Packages



(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions
   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

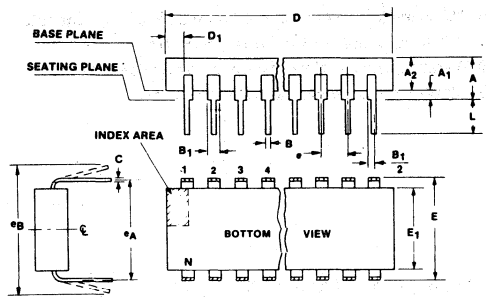
(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

92CS-39997

Dual-In-Line Plastic Packages

(E) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

Notes:

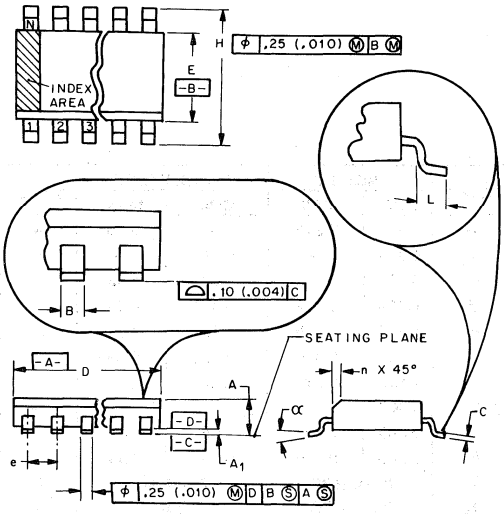
1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N, \frac{N}{2}, \frac{N}{2}+1.$$

4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

13

Dual-In-Line Small-Outline Plastic Packages



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

M Suffix (JEDEC MS-012AB)
14-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
∝	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38924R2

M Suffix (JEDEC MS-012AC)
16-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
∝	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38925R2

M Suffix (JEDEC MS-013AC)
20-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
∝	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38926R2

M Suffix (JEDEC MS-013AD)
24-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
∝	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-39037R2

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